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Executive Viewpoint - Impact of CHIPS Act will Depend on Verification

Maheen Hamid, COO, Breker Verification Systems and ESD Alliance Governing Council Member

The CHIPS Act is an effort by the U.S. government to regain control in the semiconductor supply chain and an opportunity for companies supplying chip design verification tools. In the last 20 years, the U.S. production of chips has dropped from 37% to a mere 12%. As demand for chips is not expected to abate anytime soon, the supply chain issues of the pandemic era laid bare the necessity of such an investment in our domestic industry. Two-hundred billion of the $280 billion fund is earmarked for scientific R&D and commercialization. Another $3 billion is set aside for leading-edge technology and the wireless supply chain. Investing in advanced thought leadership in chip design and translating those into advantages in the manufacturing processes is the only way to leapfrog ahead of current competitive gains held by foreign manufacturing giants. It is notable that these investments lead to knock-on advances in design excellence such as Intel's "System Foundries."

To realize any such paradigm shifts in design complexity, be it through academic research or private industry investments, high-coverage verification at the system level is critical. Many of the tax incentives related to private industry's qualified investments in chip manufacturing will disappear on January 1, 2027. This is the time to try fast, fail fast and that's where technologies such as Breker's test suite synthesis and System Verification Intellectual Property (SystemVIP) libraries can become a catalyst in the process. Allowing verification knowledge capture early in the cycle and scaling as design modules are added, test content generation from simulation to post-silicon ceases to be a bottleneck. It can also enable creation of leading-edge designs necessary to recapture the market dominance envisioned by this fund.

About Maheen Hamid

Maheen Hamid is a recognized entrepreneur and co-founder of Breker Verification Systems, a chip design verification company where she serves as COO and CFO. Maheen is a member of the ESD Alliance Governing Council.

The Design and Verification Ecosystem's Place in the CHIPS Act

Bob Smith, Executive Director, ESD Alliance

2023 is shaping up to be a year of major changes that are rippling through the global semiconductor industry. The shakeup and reordering of established supply chains are quite visible and being driven in large part by geo-political issues. Many countries have now committed to investing in their own domestic semiconductor design and manufacturing capabilities.

In the U.S., the CHIPS Act is moving at full speed with the creation of the National Semiconductor Technology Center (NSTC) as a central organization under the Commerce Department. It will play a large role in where CHIPS Act funding is applied. In parallel to the CHIPS Act, there is already substantial private capital flowing into the planning and construction of multiple new leading-edge semiconductor fabrication facilities in the U.S. For all of us in the design and verification ecosystem, it is great to see the semiconductor industry being in the spotlight as a critical industry for the future.

Where does the design and verification ecosystem fit within the context of the CHIPS Act? Most articles covering the CHIPS Act focus on the re-building our domestic semiconductor manufacturing capability. This leaves us to wonder where our segment of the industry would fit.

If we dig a little deeper and look at the CHIPS R&D vision, we find three important pillars:

- Ensure that the U.S. invents, develops and deploys the foundational semiconductor technologies for the future.
- Create a domestic semiconductor ecosystem that focuses on getting the best ideas to commercial scale quickly and cost effectively.
- Invest in building the skilled workforce for the future that will be needed to support the domestic semiconductor ecosystem.

A topic that is high on the list under foundational technologies is investment in "More than Moore" design and manufacturing capabilities using chiplet-based design and heterogeneous integration. In recommendations made to Commerce and the NSTC, there is an expressed need for new design automation and verification technologies and tools to enable this transition to the next generation of systems design. This is one visible point where our industry will play an important role in the ultimate mission of the CHIPS Act.

News Briefs

ESD Alliance Export Seminar — The Impact of New Regulations on EDA and SIP
Ada Loo, chair of our Export Committee and Group Director and Associate General Counsel at Cadence Design Systems, will host an export seminar on the impact of new regulations on the electronic systems design ecosystem. The breakfast meeting will be held Tuesday, March 28, from 8:30am until 11:30am at Cadence's corporate headquarters in San Jose.

The session will feature the Cadence Government and Trade Group addressing general trade compliance concepts, how export control and sanction regulations affect the industry and current trends and emerging issues. Audience questions will be encouraged.

Speakers are Ada Loo and William Duffy, Cadence's Corporate Counsel.

Member tickets are $100 each and $125 per non-member. Member pricing is offered for individuals or companies that are active SEMI members. Visit the ESD Alliance website to register: www.esd-alliance.org.

SSCP Continues Moving Through Certification Process
The ESD Alliance and SEMI will soon announce the latest news on the anti-piracy SEMI Server Certification Protocol (SSCP) for software license management as it moves through SEMI's standardization process. Created through the efforts of development committee members Cadence, Siemens EDA and Synopsys, the goal is to make it an industry standard approach to help protect against unlicensed usage of software licenses. To learn more about SSCP, contact the SEMI ESD Alliance at info@esd-alliance.org.

Get to Know the ESD Alliance, a SEMI Technology Community
We're the ESD Alliance, a SEMI Technology Community, representing members in the electronic system and semiconductor design ecosystem focusing on technical, marketing, economic and legislative matters affecting the entire industry. Formerly known as the Electronic Design Automation Consortium (EDA) or EDAC, we are the central voice to communicate and promote the value of the semiconductor design ecosystem as a vital component of the global electronics industry.

Much of our member value is derived from the various technical- and business-oriented committees whose members are subject matter experts from our member companies. These initiatives address key areas of common concern for our industry — Risk Management, Growth and Efficiency, Market Information, Events and Education, the Phil Kaufman Award and the Phil Kaufman Hall of Fame.

Visit Members' Booths at DVCon:
Breker (#112), Cadence (#114), Real Intent (#129), S2C, Siemens (#113), Sigasi (#130), Synopsys (#105-107)

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