

SEMI AROUND THE WORLD

Toepper of Fraunhofer Institute Receives European SEMI Award

Dr. Michael Toepper of the Fraunhofer Institute "Reliability and Microintegration", Berlin, Germany, was honored with the European SEMI Award for 2007 for his leadership in the BCB-based redistribution technology in advanced wafer level packaging.

Toepper played a key role in implementing the concept of wafer level packaging into manufacturing, which required significant research on materials and process technology.

"Today, the chip package is no longer a commodity. As a result of a number of bright ideas and innovations, it is an enabler for the interconnectivity of integrated systems," said Heinz Kundert, president, SEMI Europe. "SEMI is honored to grant the European SEMI Award to one of the greatest innovators in the field of packaging."

Toepper received a Ph.D. in material science from the Technical University of Berlin in 2003. In 1999 he became the head of a research group at the Fraunhofer IZM Institute, which specializes in advanced packaging. He has authored and co-authored more than 130 papers related to electronic packaging and currently chairs the IEEE Technical Committee of Wafer Level Packaging. •

300 mm, Memory Main Drivers For Fab Spending

300 mm fabs and memory are expected to be the main growth drivers for fab spending, and 85 percent of all fab spending will go toward equipping 300 mm fabs in 2007, according to the recently updated *FabFutures* report released by SEMI.

This year, a total of about 23 million 8-inch equivalent wafers of new capacity has been added; up 16 percent from the previous year. The two fastest-growing segments are for memory-type fabs and 300 mm fabs in general.

Capacity of all memory fabs increased 33 percent from 2006 compared to 51 percent from 2005 to 2006. The total capacity of all 300 mm fabs is expected to increase by over 50 percent from 2006 to 2007. •

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SEMICON West Shines

FOR MORE THAN 35 YEARS SEMICON® West has been the place to find everything and everyone connected to the world of semiconductor manufacturing, and in recent years, nanoelectronics. At SEMICON West 2007, scheduled for the Moscone Center, San Francisco, July 16–20, you'll find innovations, information, products, and people focused on the design and manufacture of semiconductors, nanoelectronics, MEMS, and renewable energy applications such as solar and fuel cell technology.

The Expo has become the venue of choice for showcasing new products and technologies and for the exploration and introduction of emerging technologies. Virtually every new major semiconductor manufacturing technology over the past 30 years debuted at SEMICON West. This year, over 170 of the 1,180 exhibiting companies will introduce more than 200 new products at the show.

One of the most popular SEMICON West events over the past several years has been the TechXPOTs ("Tech Spots"), featuring a combination of exhibits, live technical content, and presentations by the winners of the Technology Innovation Showcase (TIS). This year's TechXPOTs include Emerging Technologies & Markets, Test Assembly & Packaging and Challenges in Device Scaling. In five sessions over three days, show attendees find out what's moving next generation applications, manufacturing technology and materials. All TechXPOT presentations are free-of-charge to registered visitors.

SEMICON West 2007 highlights include:

DAILY KEYNOTES: Insightful and topical presentations given by high-level executives from device makers such as AMD, Cypress Semiconductor, Intel, and EDA leader Synopsys.

TEST SUMMIT: CEOs from Advantest America, Credence, Nextest, Teradyne

and Verigy will join in a discussion focused on meeting the design, test, and yield requirements for advanced semiconductor manufacturing.

SOLAR/PHOTOVOLTAICS:

No topic is hotter right now than renewable energy, and applications from PV to fuel cells represent new markets and opportunities for growth. SEMICON West offers a variety of programs and events to spotlight this exciting technology.

BULLS AND BEARS: This forum provides attendees with an equities market perspective on the first six months of the year, and a look ahead at the rest of the year. Panelists include leading investment and equities analysts.

ITRS: The International Technology Roadmap for Semiconductors (ITRS) will conduct a public meeting at SEMICON West on July 18. Opportunities for networking, electronic posters, and Q&A will be part of the public interaction.

If that's not enough, SEMICON West 2007 also features a used equipment forum, the Chemicals & Gases Manufacturers Group general meeting (open to the public), SEMI market symposium, EHS meetings to discuss the continuing impact of RoHS and REACH legislation, short courses and workshops on various technical subjects, and SEMI standards program meetings.

I believe that trade shows remain the most efficient and cost-effective way to communicate with a broad range of audiences. Certainly, the trade show model has evolved from the days where companies displayed physical examples of their latest products. In today's mobile and interconnected world, that's obsolete. However, face-to-face marketing is still a vital part

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SEMI STANDARDS

SEMI Publishes Six New Technical Standards Including Guidelines for FPDs, SOI Wafers

SEMI HAS PUBLISHED SIX NEW TECHNICAL STANDARDS

applicable to the semiconductor, flat panel display (FPD) and MEMS manufacturing industries. The new standards, developed by technical experts from equipment and materials suppliers, device manufacturers and other companies participating in the SEMI International Standards Program, are available for purchase in CD-ROM format or may be downloaded from the SEMI website, www.semi.org.

SEMI Standards are published three times a year. The new standards, part of the June 2007 publication cycle, join more than 740 standards that SEMI has published during the past 34 years.

"These new SEMI standards, which include specifications for the flat panel display (FPD) manufacturing industry, are the result of collaborative, consensus-driven efforts among industry experts — competitors and customers alike — to manage the ever increasing manufacturing challenges, to improve yield and to ensure compatibility of equipment and processes worldwide," said Bettina Weiss, SEMI director of International Standards.

The new standards include specifications for bar code container identification, specifications for silicon-on-insulator (SOI) wafers, and a test method for surface hardness of FPD polarizing film. In addition to the six new standards, SEMI revised a previously published standard on EHS guidelines for exhaust ventilation of semiconductor manufacturing equipment. The revised SEMI S6 offers significantly more detailed guidance and provides equipment suppliers, evaluators and users a means of validating the adequacy of exhaust ventilation.

The new standards include:

SEMI C61

Specification for Bar-Code Container Identification

SEMI C61 applies to warehousing/manufacturing processes where packaged chemicals or isotainer (bulk) chemicals are being handled and where empty returnable containers need to be tracked.

Device makers are confronted with supplier-specific bar-code identification techniques on chemical containers, which complicates the development and usage of automated tracking and control applications at the manufacturing site. On the other hand, suppliers are being asked by device makers to develop customer-specific bar-code container identification solutions that also complicate the product labeling process and generally increase inventory costs.

This standard will allow device makers to build automated control applications that are independent of the supplier. The benefits of this approach include faster design, development and implementation and lower software development costs. For suppliers, the standard will allow them to bar-code their products independently of where the product eventually will be shipped. This means their product labeling process becomes simpler, which translates into lower software development and maintenance costs.

SEMI D49

Specification of Single Substrate Orientation for Loading/Unloading into/from Equipment to Specify ID Reader Position

SEMI D49 is used in FPD manufacturing. It clarifies the reading position of the substrate ID during the load/unload between the AMHS and equipment by specifying the orientation of the single substrate against the equipment opening.

Application of this standard improves the communications among panel makers, equipment suppliers, and AMHS manufacturers and subsequently reduces the time taken for on-site installation and adjustment of the reader. In addition, standardizing ID reading positions increases the ID reading accuracy, which is an essential element for traceability.

SEMI D50

Test Method for Surface Hardness of FPD Polarizing Film

The ISO standard 15184 for determining the hardness of coating films has been adopted for measuring the surface hardness of FPD polarizing film and its materials. SEMI D50 clarifies the differences when evaluating a polarizing film and its materials.

It defines the procedural guideline for measuring the surface hardness of a polarizing film and its materials for FPD production. These procedures are applicable to manufacturing, quality control, and development work.

SEMI E148

Specification for the Definition of Time Synchronization Method and Format

SEMI E148 solves the time synchronization and time stamping issue with equipment data quality and the problem of being able to accurately collect time-based data. Accurate timestamps reduce the time needed to study and to correlate events to solve process

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Critical Issues in Test Highlighted at TechXPOT Session

THE TEST EQUIPMENT INDUSTRY needs to leapfrog their customers in order to add value to the semiconductor manufacturing supply chain, according to a speaker scheduled to appear at the Test, Assembly & Packaging TechXPOT at SEMICON West 2007.

“We need to look a few steps ahead of the customers and understand where they are going to be in one or two Moore’s Law generations,” said Itzik Goldberger, vice president of strategy and business development, Credence Systems Corp.

In the memory test segment, flash memory bit densities are now doubling even faster than Moore’s Law. According to Hwang’s Law, named after Samsung president Hwang Chang-gyu, the density of the top-of-the-line flash memory chips will double every 12 months, said another scheduled TechXPOT speaker, Erik Volkerink, chief scientist, Verigy. The expectation is that the test industry will enable test cost to scale with the semiconductor technology progress, he said.

Goldberger of Credence believes IC manufacturers are addressing test bottleneck and cost issues better than the test suppliers right now by putting more testability onto the device and reducing the need for a test platform. “Given that trend, suppliers need to change the way we think about the value that we add,” he said.

The test industry faces many technical challenges, noted Volkerink of Verigy. Next-generation silicon technology allows integration of more and more transistors per wafer, which translates to a lower manufacturing cost per transistor because manufacturing is inherently a lithographic concurrent process. “The challenge for test is that test is not (yet) inherently concurrent; test times and cost may increase rapidly unless novel test solutions are researched and commercialized,” he said.

In addition, new silicon technologies allow ever-increasing interface frequencies and performance targets which challenge the ATE both in terms of enabling an interfacing path as well as processing capabilities. Another challenge relates to yield learning. “As we go to the next technology node, yield learning becomes more challenging. There is an opportunity for the ATE industry to introduce technologies that help customers with the yield ramp,” explained Volkerink.

Next-generation integration technology is another challenge. More and more digital logic coexists with analog and RF cores, with passives, high-voltage power, sensors and actuators, and even bio- and micro-fluidics. On top of the integration of diverse cores in one die, SIPs (System in Package) allow a continuing increase in the number of dies integrated in the same package. Test capabilities must keep pace, accommodating the diverse set of technology cores or dies.

Goldberger of Credence believes there are three elements that could provide a

solution to the challenges facing test. The first is to develop a roadmap outlining a portfolio of instruments that will be comprehensive enough to cover all current needs of the device makers as well as their anticipated needs in future. “They don’t have time to wait for technology development ... test suppliers should be ready in time for whatever their customers need in the future,” he said.

The second element is an infrastructure that allows easy scaling and changes when introducing new instruments into the platform. “That means a scalable platform and it means a plug-and-play style installation and integration,” said Goldberger.

The third part of the solution would be a powerful program development environment to reduce the time-to-market of test program development. “Our customers will continuously need to improve their ability to generate test content from EDA tools and quickly convert them into a test program,” he added.

The TechXPOT session focusing on test will be held from 3:00pm to 5:00pm on July 17. In addition to the speakers from Credence and Verigy, other presenters include Octavio Martinez, director of Test Engineering, Qualcomm; Gary Fleeman, director, Product Engineering, Advantest; Ken Harvey, senior product technologist, Teradyne; and Colin Ritchie, vice president of Marketing, Inovys. •

marks the XPOT
Explore what’s new and what’s next
in micro- and nanoelectronics
at the TechXPOTs.

“As soon as the industry anticipates a new test cost bottleneck, it innovates and introduces new technologies to address the bottleneck. In the aggregate, those innovations attempt to make test cost scale,” said Volkerink. For example, in the logic test segment, new test compression technologies help control logic test cost. As another example, in the memory test segment Verigy’s tester-per-pin technology enables high frequency capabilities at a relatively low cost point. The same technology addresses the multi-core nature of SOC and SIP devices by allocating tester resources to each port as needed to exactly match the test needs of the core.

PERSPECTIVES *continued*

of maintaining business relationships and influencing the perception of important buyers and specifiers. Anyone can send data sheets and price lists to a customer; but only a trade show uses sight, sound and all the senses to effectively position products and frame buying decisions. That’s where SEMICON West shines.

— Stan Myers •



SEMI STANDARDS *continued*

problems. By synchronizing the equipment and applications during the manufacturing process, users can correlate data from multiple sources in the factory and take action in a timely and confident manner.

In the near future SEMI E148 promises to raise the quality of the data stored by the manufacturing systems and enable more automated decision-making tools. This standard enables the merging of manufacturing data from multiple sources to provide a broader understanding of what is actually occurring on the manufacturing floor.

SEMI E149 **Guide for Documentation** **Provided to the Equipment User** **for Use with Semiconductor** **Manufacturing Equipment**

SEMI E149 applies to the purchase of semiconductor or FPD manufacturing equipment. Prior to this document, no single SEMI standard defined all of the content and related requirements (such as operation, maintenance, and installation manuals) provided by the equipment supplier. However, some SEMI standards do cover equipment documentation content requirements for a few areas, such as SEMI E6 for installation manuals and SEMI S13 for EHS-related documentation.

The E149 standard will save negotiating time for purchasers and equipment suppliers by providing minimum documentation requirements. It will also support more effective equipment negotiations and purchase agreements between the equipment supplier and purchaser/user.

SEMI M71 **Specification for Silicon-on-Insulator** **(SOI) Wafers for CMOS LSI 130 nm** **Technology Generation and Beyond**

SEMI M71 relates to the selection and purchase of SOI wafers for VLSI applications. It simplifies the process of purchasing SOI wafers by clarifying communication between the wafer suppliers and their customers and helps in preventing

confusion and misunderstanding that might lead to incorrect specifications and to purchasing of wafers that are not suitable for the planned application.

Since the standard improves communication between both parties, it reduces the costs associated with the sales transactions. The vendors will be better informed as to which parameters need to be specified and the most efficient method of describing their products. The customers will receive a better understanding of how to select the wafers they require.

SEMI S6 **EHS Guideline for Exhaust** **Ventilation of Semiconductor** **Manufacturing Equipment**

SEMI S6 is directly related to the exhaust ventilation aspects of semiconductor manufacturing equipment, but can be applied to FPD and MEMS manufacturing environments.

Although this is a revision of an existing SEMI standard, it provides significantly more detailed guidance and addresses issues related to design and performance criteria, validation, and reporting. It includes appendices containing test methods and several related information sections, such as general design recommendations.

By providing performance, design and validation criteria that are commonly accepted by equipment suppliers, evaluators and users, SEMI S6 should reduce design costs for "off-the-shelf" equipment. It should also reduce the number of safety related "customer special" design requirements.

Semiconductor manufacturing equipment relies heavily on exhaust ventilation to maintain a safe working environment. However, previously there were no industry consensus standards or design guides that specifically address this type of equipment. The revised SEMI S6 fills this gap and provides equipment suppliers, evaluators and users a means of validating the adequacy of exhaust ventilation. •

CALENDAR OF EVENTS

AUGUST 2007

August 16
Silicon Valley Lunch Forum
Santa Clara Marriott
Santa Clara, California
www.semi.org/svlf

SEPTEMBER 2007

September 4-5
SEAJ/SEMI Industry
Strategy & Technology
Forum
Pacifico Yokohama
Yokohama, Japan
www.semi.org

September 12-14
SEMICON Taiwan 2007
Taipei World Trade Center
Taipei, Taiwan
www.semi.org/semicontaiwan

September 19
New England Breakfast
Forum
Woburn, Massachusetts
www.semi.org/

OCTOBER 2007

October 9-11
SEMICON Europa 2007
Stuttgart, Germany
www.semi.org/semiconeuropa •

SEMI AROUND THE WORLD

First Quarter Equipment Billings **Up 12 Percent Year-on-Year**

Worldwide semiconductor manufacturing equipment billings reached \$10.75 billion in the first quarter of 2007, four percent higher than the fourth quarter of 2006 and about 12 percent above the same quarter a year ago, according to SEMI data gathered in cooperation with the Semiconductor Equipment Association of Japan (SEAJ).

SEMI also reported worldwide semiconductor equipment bookings of \$10.50 billion in the first quarter of 2007; six percent above the same quarter a year ago and five percent below the bookings figure for the fourth quarter of 2006.

"Billings for the first quarter of 2007 posted slight gains over the fourth quarter of 2006, with Korea showing particularly robust growth," said Stanley T. Myers, president and CEO of SEMI. "Year-over-year sales were largely mixed, with China, Korea and Taiwan posting solid double-digit growth numbers." •