Wednesday, May 15, 2013 (Day Two)

7:30 Registration

8:30 **Keynote: Fab Materials Next Generation Challenges: Affordability & Quality**
Tim Hendry, Vice President, Technology and Manufacturing Group, Director of Fab Materials, Intel Corporation (sponsored by CNW)

Session 6 Yield Enhancement I (sponsored by FEI Company)
Chairs: Oliver Patterson, IBM; Gary Green, Alphray

Defect inspection, yield analysis and optimization are integral components in the development and manufacture of semiconductor devices. This session covers a variety of techniques to improve yield using design, defect, electrical test, bitmap and failure analysis data. Using two or more of these data sources together intelligently is a recurrent theme.

9:05 6.1 Effective Co-optimization of DFM and Defect Inspection Methods for Fast Yield Ramp
Yan Pan, Rao Desineni, Jane Lambert, Edward Teoh, Victor Lim, Goh Szu Huat, Thomas Berndt, GLOBALFOUNDRIES; John Kim, Sagar Kekare, Synopsys

9:30 6.2 Use of Performance Path Test to Optimize Yield
Jeanne Paulette Bickford, Jinjun Xiong, IBM

9:55 Break

10:15 6.3 Statistical Correlation of Inline Defect to Sort Test in Semiconductor Manufacturing
Uwe Hessinger, Brett Schafman, Wendy Chan, Toan Nguyen, Shiree Burt, Lattice Semiconductor Corporation

10:40 6.4 Heading Towards Big Data: Building A Better Data Warehouse For More Data, More Speed and More Users
Raymond Goss, Kousikan Veeramuthuk GLOBALFOUNDRIES

11:05 6.5 Case Studies of Fault Isolation for the Global Failing Patterns on SRAM Bitmap caused by the Defects in Peripheral Logic Regions
Jianhua Yin, Jian Yu, Sheng Xie, Dapeng Sun, Yong Ern Ling, GLOBALFOUNDRIES; Zhigang Song, Carl E. Schiller, Genadi Teverskoy, Manuel J. Villalobos, IBM

11:30 Boxed Lunch