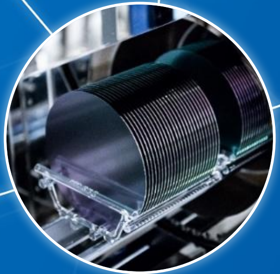


Artificial Intelligence

5G

# SOITEC
## Engineered Substrates and Materials for 5G (B5G & 6G)

Cesar Roda Neve - 18th Nov. 2021


Energy Efficiency

# Outline

1. About Soitec technology
2. 5G / B5G & 6G system needs
3. Existing and NEW materials
4. Takeaways & Conclusions

1

# Soitec technology

soitec

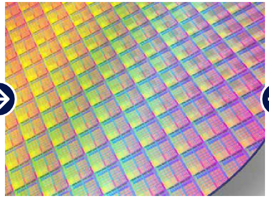
# Soitec has built a unique position in the value chain…

soitec

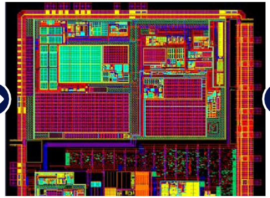
LEADING SUPPLIER

BULK MATERIALS

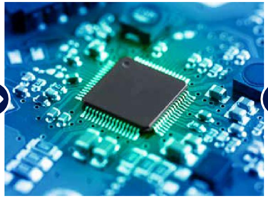
ENGINEERED SUBSTRATES



FOUNDRIES |



DESIGN |



FABLESS

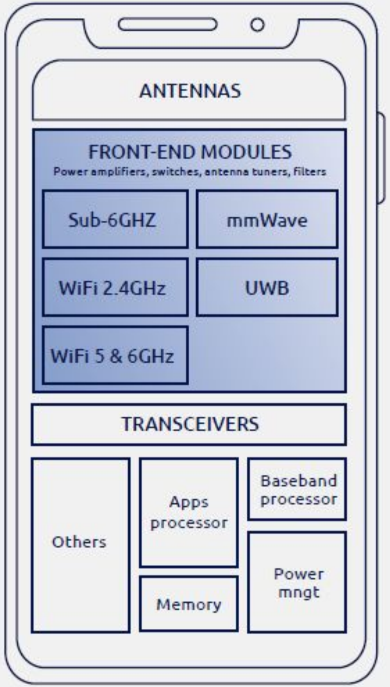
END MARKETS

MOBILE COMMUNICATIONS

AUTOMOTIVE & INDUSTRIAL

# A COMPREHENSIVE OFFER FOR
# RF AND mmWave FRONT END MODULES

soitec

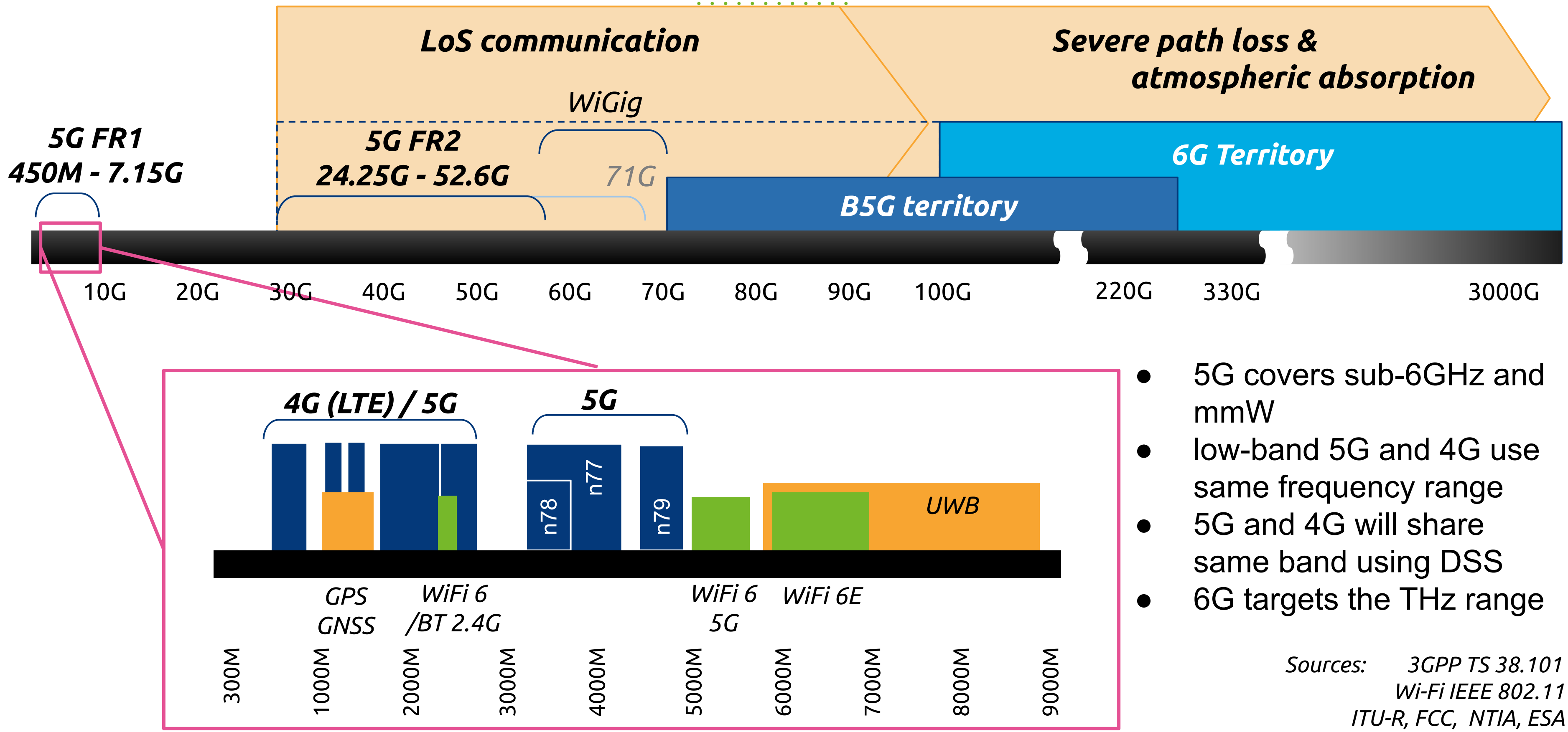



| | | POWER AMPLIFIER (PA) | LOW NOISE AMPLIFIER (LNA) | SWITCH | ANTENNA TUNER (AT) | FILTER | ENVELOPE TRACKER (ET) | PHASE SHIFTER | SYSTEM ON CHIP (SoC) |
|---|---|---|---|---|---|---|---|---|---|
| 4G / 5G SUB-6GHZ FEM KEY BLOCKS | RF-SOI | □ | ■ | ■ | ■ | □ | □ | □ | □ |
| | POI | □ | □ | □ | □ | ■ | □ | □ | □ |
| | FD-SOI | □ | □ | □ | □ | □ | ■ | □ | □ |
| | GaN | ■ | □ | □ | □ | □ | □ | □ | □ |
| 5G MMW FEM KEY BLOCKS | RF-SOI | ■ | ■ | ■ | □ | □ | □ | ■ | □ |
| | FD-SOI | □ | □ | □ | □ | □ | □ | ■ | ■ |
| | GaN | ■ | ■ | □ | □ | □ | □ | □ | □ |
| WIFI & UWB FEM KEY BLOCKS | RF-SOI | ■ | ■ | ■ | □ | □ | □ | □ | □ |
| | POI | □ | □ | □ | □ | ■ | □ | □ | □ |
| | FD-SOI | □ | □ | □ | □ | □ | □ | ■ | ■ |

2

# 5G / B5G & 6G system needs

# 5G/B5G/6G/WiFi/BT Spectrum




- 5G covers sub-6GHz and mmW
- low-band 5G and 4G use same frequency range
- 5G and 4G will share same band using DSS
- 6G targets the THz range

*Sources: 3GPP TS 38.101*
*Wi-Fi IEEE 802.11*
*ITU-R, FCC, NTIA, ESA*

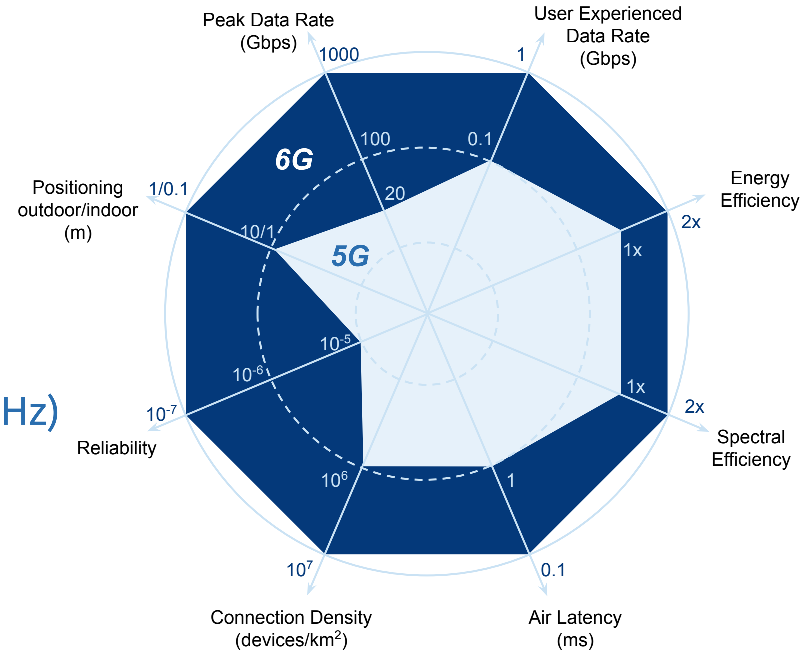
# System needs for 5G / B5G & 6G

**5G**

- Spectrum extension up to mmW
- High RF power
- Energy efficiency
- High linearity
- High RFFE integration

**B5G & 6G**

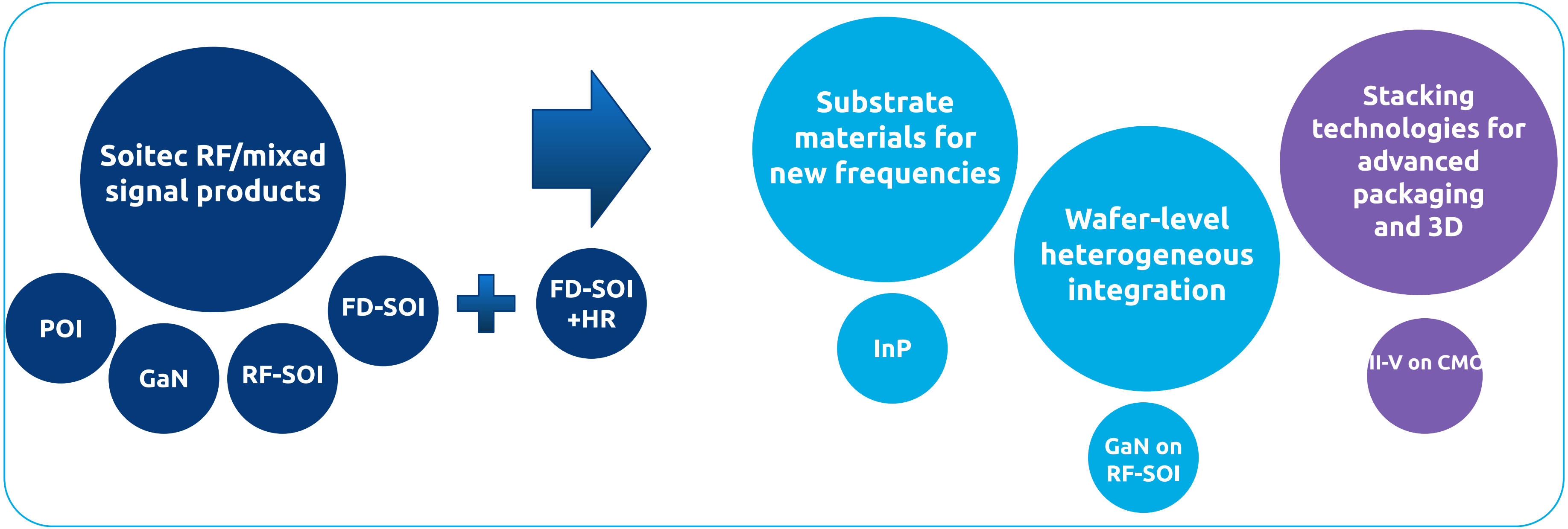
- More efficient use of new and existing spectrum (up to THz)
- More efficient use of radiated RF power
- Excellent linearity
- High speed I/Os, DAC/ADC
- System integration of best in class technologies (RFFE, analog/mixed, processing)




*Source: Samsung research , 2021*

# New substrate materials for 5G / B5G & 6G

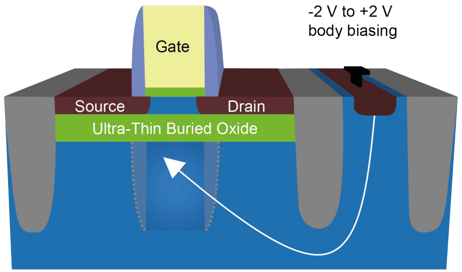
- Use of existing high-performance solutions
- Enhancement of current 4G/5G solutions for mmW and 6G
- New substrate materials for B5G and 6G
- New substrate materials for higher performance in 5G applications



3

# Existing and NEW Materials

# FD-SOI for 5G mmW




- FD-SOI gives superior power/performance tradeoff
- Smaller process variability
- Better analog/RF performance
  - Higher bandwidth/lower power
  - Lower noise
  - Less parasitics
- mmW FEW building blocks show excellent performance
- Ideal for SOC integration with mmW FEM

*28 GHz FEM Benchmark* circuit results (SOI 22FDX)*

| | | | | |
|---|---|---|---|---|
| | **Peak PAE** | **Psat** | **Gain** | **3dB BW** |
| **PA (differential cascode)** | 42% | 18 dBm | 13 dB | 11 GHz |
| | **Gain** | **IIP3** | **NF** | **Pdc** |
| **LNA (single stage cascode)** | 13 dB | 3 dBm | 1.35 dB | 13 mW |
| | **IL** | **Isolation** | **OIP3** | |
| **Switch (3-stack series/shunt)** | 0.65 dB | > 23 dB | >30 dBm | |

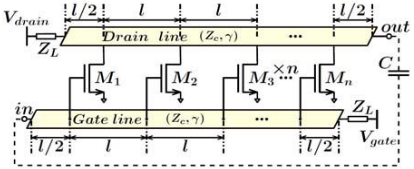
*FD22X → ft/fmax: 350/430 GHz*

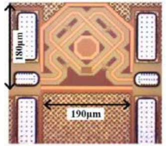
*Source: Global Foundries , 2021*

**Benchmark results in-line with state-of-the-art results (see Annex)*

# FD-SOI already a solution for >100 GHz

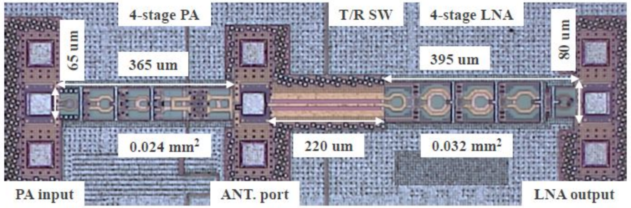
***Distributed oscillator at 134 and 202 GHz***
***28 nm FD-SOI CMOS***



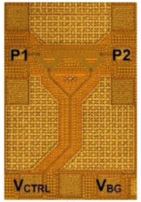

***Ref: R. Guillaume at al, RFIC'17***

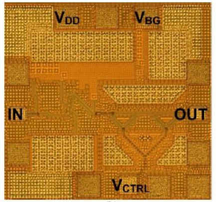
***140 GHz T/R Front-End Module in 22 nm FD-SOI CMOS***




***Ref: Xinyan Tang etal, IMS'21***

***220 GHz high-isolation SPST switch and Voltage Gain LNA***



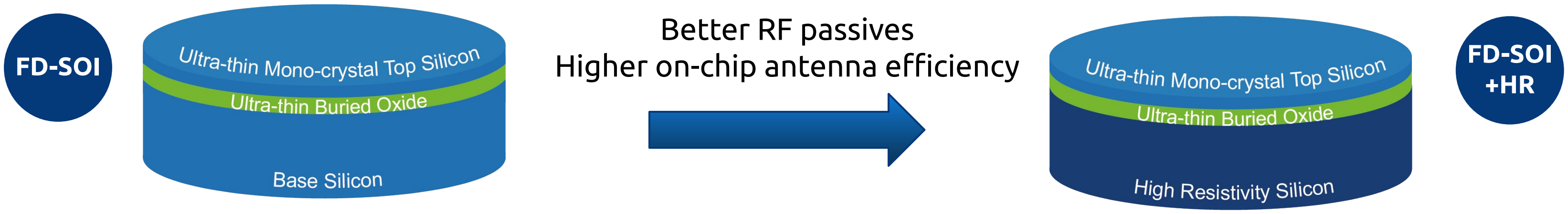



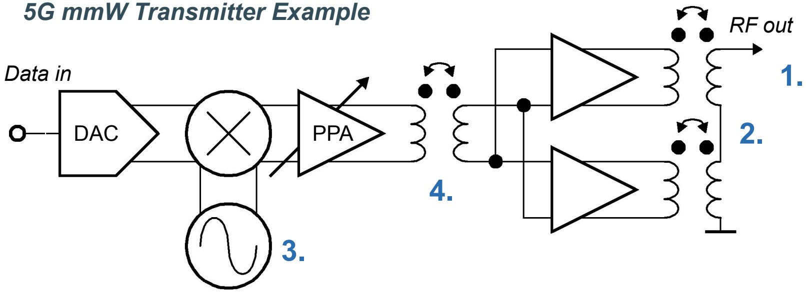

***Ref: Lucy Wu, IMS'21***

**FD-SOI: SoC TECHNOLOGY FOR Co-INTEGRATED LOGIC & RF FEM SYSTEMS (5G/mmW)**

# FD-SOI Material Roadmap

## Addressing both Next-Generation 5G mmW & Sub-THz design



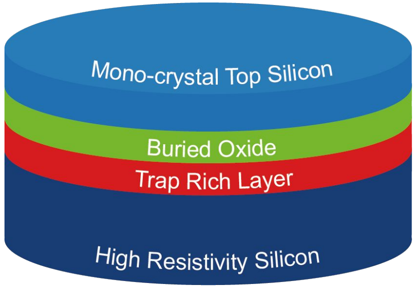




### Blocks to potentially benefit from FD-SOI+HR

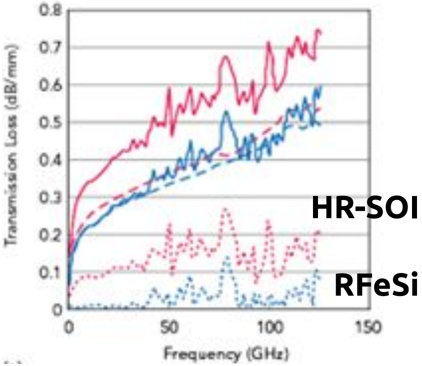
1. RF Switch Performance
2. RF Output Power Combining
3. Synthesizer Phase Noise
4. RF Inter-stage Matching
5. RF Phase Shifter (not shown)

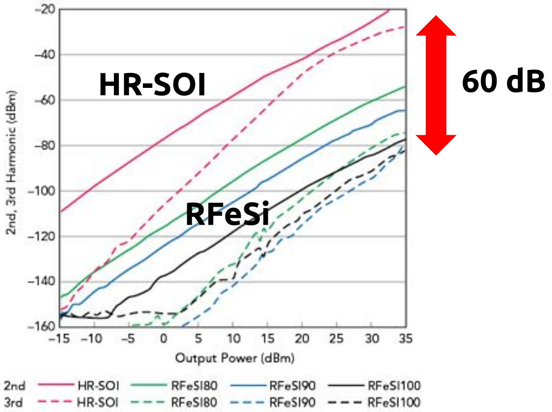
**FD-SOI +HR: SCALING OPERATION FREQUENCY WHILE MAINTAINING DIGITAL INTEGRATION**

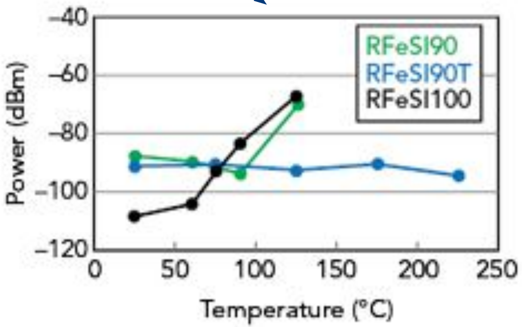
# RF-SOI for RFFE




- RFeSi substrates provide the benefit of Si CMOS and a high-resistivity substrate
- Parasitic reduction and high-speed transistors
- High-quality RF passives with improved quality factor and low-loss interconnections
- Highly linear substrate (for RF switches and passives)
- Can be enhanced to provide temperature stability



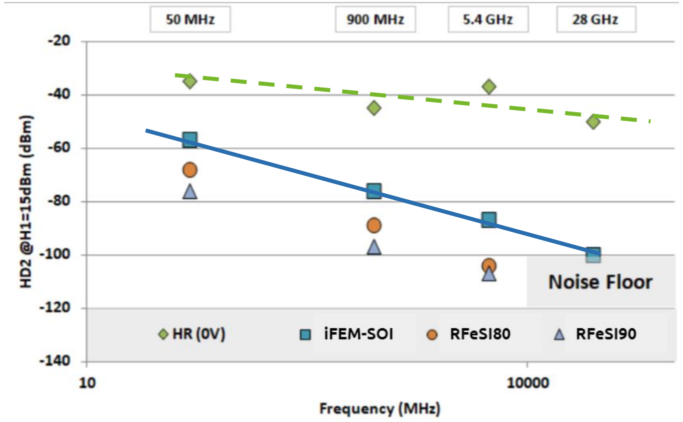



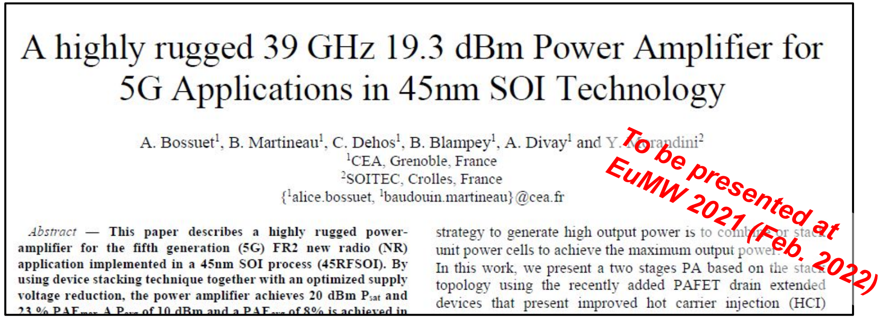

*Measurements performed in collaboration with UCLouvain*

# RF-SOI for 5G mmW

- Low substrate losses kept at > 100 GHz
- Linearity is maintained at 28 GHz
  RFeSI performs even better at mmW
- Use of transistor stacking techniques thanks to single FET isolation
- Ideal for Integration of robust high-end FEM modules at 24 and 40 GHz
  - PA
  - LNA
  - RF switches
  - envelope trackers
  - phase shifter
  - combiners




*Measurements performed in collaboration with UCL*



A highly rugged 39 GHz 19.3 dBm Power Amplifier for 5G Applications in 45nm SOI Technology

A. Bossuet[1], B. Martineau[1], C. Dehos[1], B. Blampey[1], A. Divay[1] and Y. Morandini[2]
[1]CEA, Grenoble, France
[2]SOITEC, Crolles, France
{[1]alice.bossuet, [1]baudouin.martineau}@cea.fr

*Abstract* — This paper describes a highly rugged power-amplifier for the fifth generation (5G) FR2 new radio (NR) application implemented in a 45nm SOI process (45RFSOI). By using device stacking technique together with an optimized supply voltage reduction, the power amplifier achieves 20 dBm $P_{sat}$ and 23 % $PAE_{max}$. A $P_{avg}$ of 10 dBm and a $PAE_{avg}$ of 8% is achieved in

strategy to generate high output power is to combine or stack unit power cells to achieve the maximum output power. In this work, we present a two stages PA based on the stack topology using the recently added PAFET drain extended devices that present improved hot carrier injection (HCI)



*CEA-SOITEC JDP for RF-SOI 40 GHz applications*

# RF-SOI also for > 100 GHz applications

## Beamforming phase-array transmitter at 140 GHz using 45 nm RF-SOI CMOS

8-Element 140 GHz Phased-Array Transmitter w/ 32 dBm Peak EIRP and > 16 Gbps 16QAM and 64QAM Operation

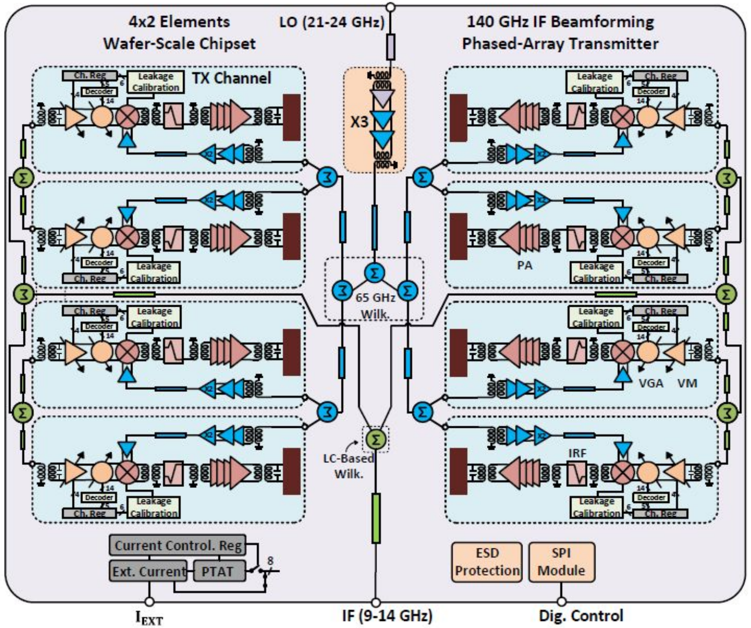
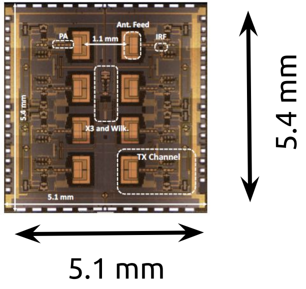
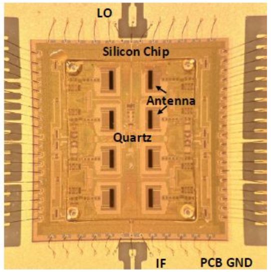



Fig. 1. Block diagram of 8-element wafer-scale IF beamforming phased array transmitter chipset at 140 GHz in CMOS-SOI.




*Ref: Siwei Li et al, RFIC'21*

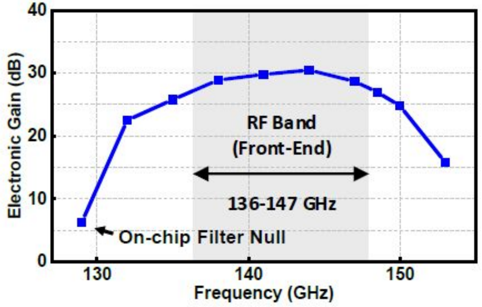



Fig. 4. Measured array electronic gain with a fixed IF frequency (11 GHz).

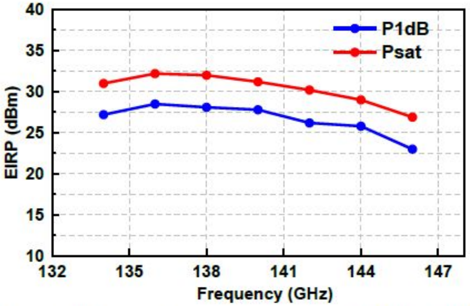
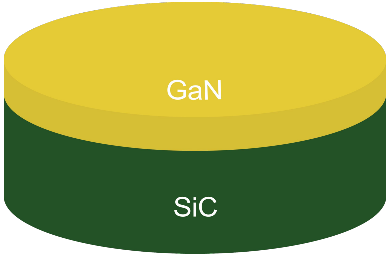



Fig. 5. Measured 8-element phased-array transmitter EIRP at P1dB and Psat versus frequency.

# GaN RF technology

**GaN RF technology is typically deployed in the sub 6GHz and X-band**

- Typically based on 20nm Al25Ga75N / GaN HEMT grown on SiC substrates
    - SiC ⇒ high-end
    - Si ⇒ low-cost
- Features very high power density (~ 10W/mm) and high PAE (>65%)
- Operated at 28V or 48V
- High temperature capability
- Typical application is in infrastructure (base stations)





# GaN RF technology for mmW

## For higher frequency operation

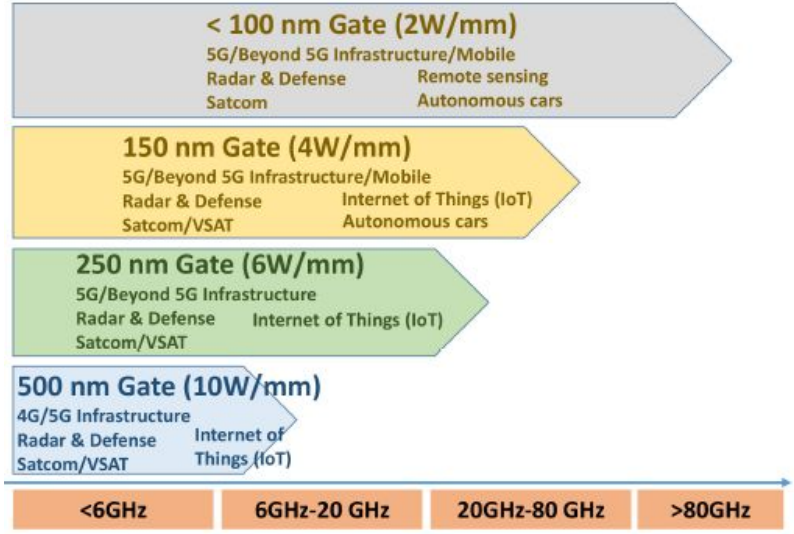
**Gate scaling**

- Lower power density and PAE

**Advanced HEMT concepts are needed**

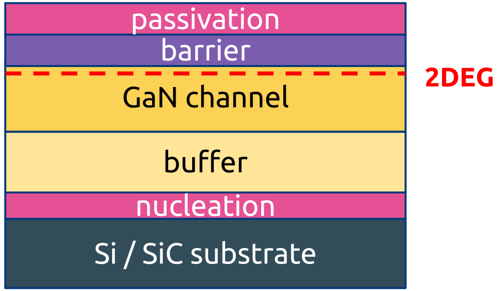
- HEMTs with very thin AlN barriers
- HEMTs with InAlN based barriers

*Possible roadmap of RF GaN HEMTs*




Source: Hsu, L.-H. et al, Micromachines 2021, 12, 1159

*HEMT epitaxial structure*

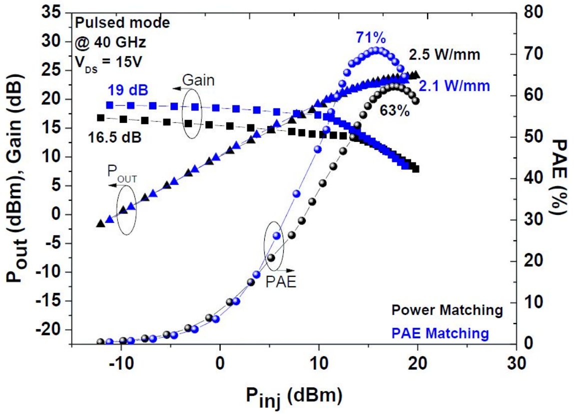


# Performance of GaN HEMT for RF PA at mmW

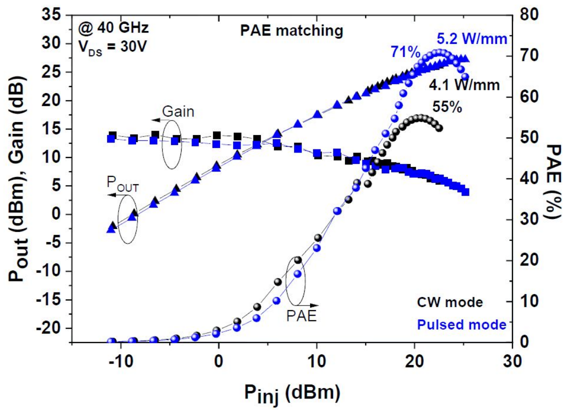
Active load-pull **@ 40 GHz**
2x50um HEMT w/ **Lg = 110nm**

Active load-pull **@ 94 GHz**
2x25um HEMT w/ **Lg 80nm**

## InAlN barrier

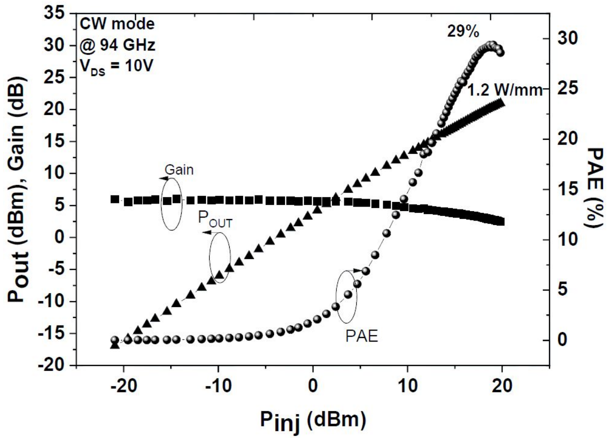



## AlN barrier




- AlN barrier robust HEMT solution with higher power density
- State-of-the-Art PAE (71%)
- InAlN having higher gain due to much larger ft/fmax
- AlN gain limited by electron mobility

## AlN barrier



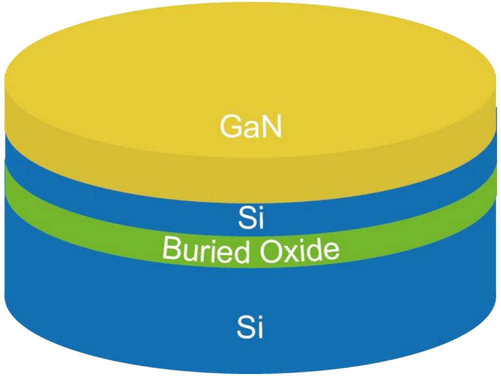

- State-of-the-Art PAE (29%) and power density
- Expected higher gain by using InAlN

***Measurements performed in collaboration with IEMN***

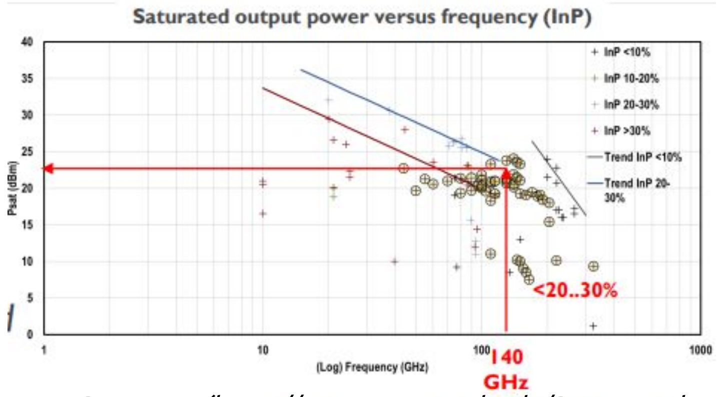
# GaN RF roadmap

## GaN on (RF-)SOI

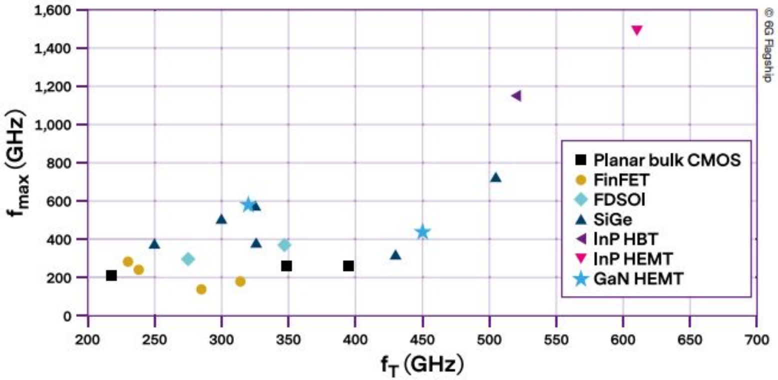
- Replace HR-Si substrate by RF-SOI
- Better vertical isolation and increased linearity
- Higher BW due to smaller feedback (vertical) capacitance
- Could allow PA, LNA and switch integration on GaN
- Possible path for Si CMOS co-integration and mobile handset application



# InP best power amplifier technology for applications > 100GHz




*Source: PA survey, (https://gems.ece.gatech.edu/PA_survey.html)*




*Source: RF Enabling 6G, 2021*

| Technology | Feature size (nm) | fMAX (GHz) | Vbr (V) | Nfmin (dB) at 50GHz** |
|---|---|---|---|---|
| GaAs pHEMT | 100 | 185 | 7 | 0.5 |
| GaAs mHEMT | 70 | 450 | 3 | 0.5 |
| GaAs mHEMT | 35 | 900 | 2 | 1 |
| InP HEMT | 130 | 380 | 1 | <1 |
| InP HEMT | 30 | 1200 | 1 | <1 |
| GaN HEMT | 60 | 250 | 20 | 1 |
| GaN HEMT | 40 | 400 | 42 | 1.2 |
| SOI CMOS | 45 | 280 | 1 | 2-3 |
| SiGe-HBT | 55 | 400 | 1.55 | 1.5 |
| SiGe-HBT | 130 | 400 | 1.4 | 2 |
| InP DHBT | 250 | 650 | 4 | 3 |
| InP DHBT | 130 | 1100 | 3 | |

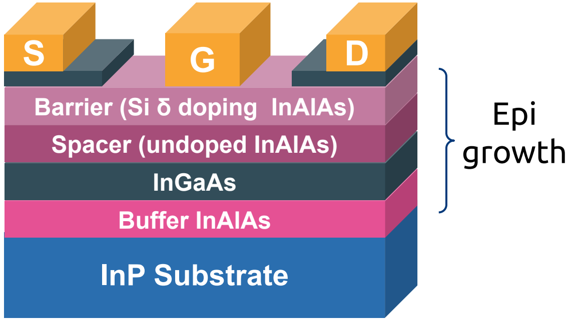
*Source: Ericsson/ST*

- A relatively mature InP 0.25um process offers fmax of 600GHz, with a breakdown voltage of 4.5V, for high efficiency with moderate output power at 140GHz
- Multistage InP PAs provide more than 20 dB of gain with efficiency of 25% @ 140GHz
- InP is superior to CMOS with higher power and higher efficiency
- InP is the only material allowing fmax at THz

# InP adoption

## InP has major advantages for RF

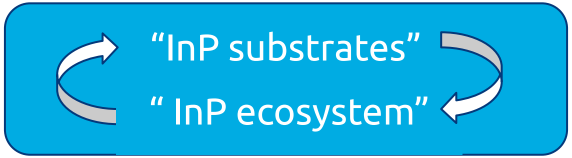
- High frequency devices (RF, THZ, 5G/6G, …)
- Very low 1/f noise
- High mobility/current gain at low current density
- Higher thermal conductivity than GaAs




*InP HEMT*

## but InP has also major drawbacks

- Expensive material
- Brittle material
- Poor availability
- Low diameter bulk substrates,
  ( mostly limited to 100 mm today)

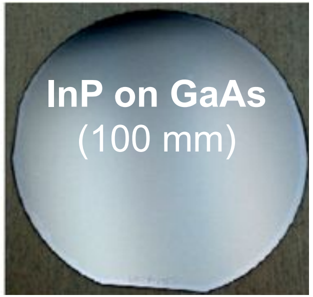



**Introduce engineered substrates solutions based on Smart Cut$^{TM}$ technology !**

# Smart Cut$^{TM}$ InP on "small diameter"

## Smart Cut$^{TM}$ "InP on Anything"

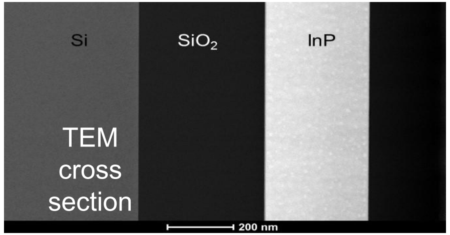
## Handle substrate

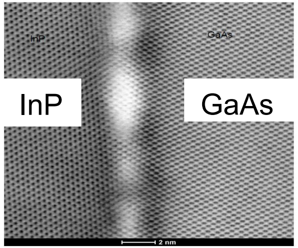


## Bonding layer

SiO2 bonding layers (InP/SiO2/Si)

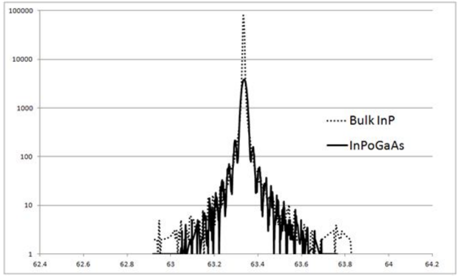



No SiO2 (InP/GaAs)




*TEM cross-section (InPOGaAs)*

## Crystalline quality





***Bibliography, see:***

*E. Jalaguier et al; IPRM 99*

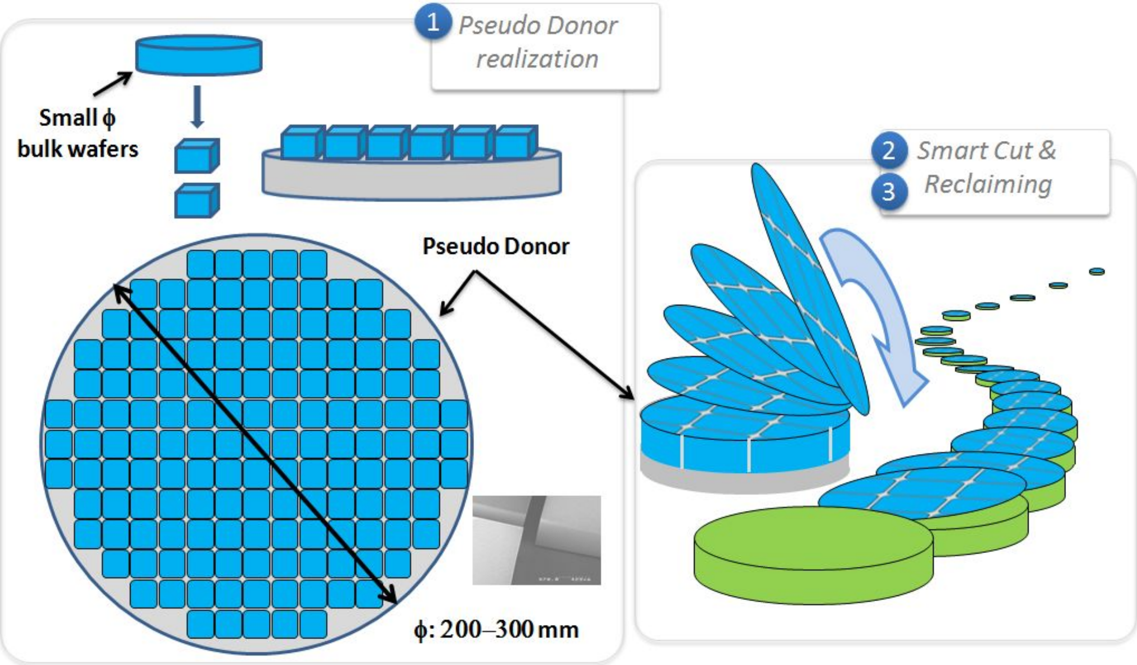
*A. Tauzin et al.; CPV 11, 2015*

*E. Guiot et al.; CSW 2015*

# Innovative InP substrate solution for 200 - 300 mm

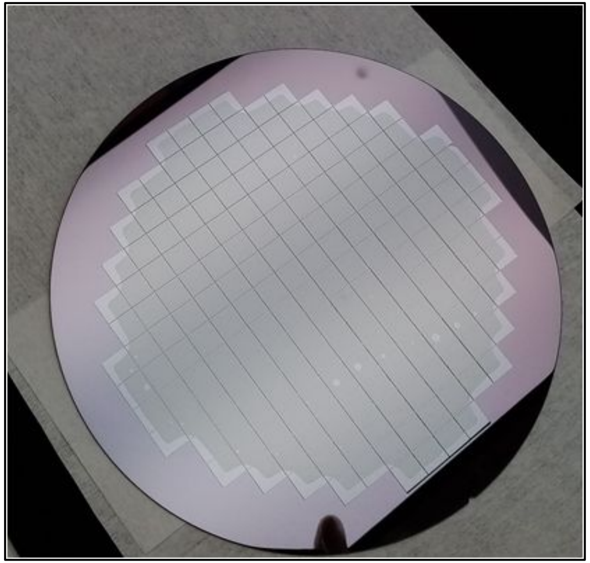
## Smart Cut™ InP & Tiling

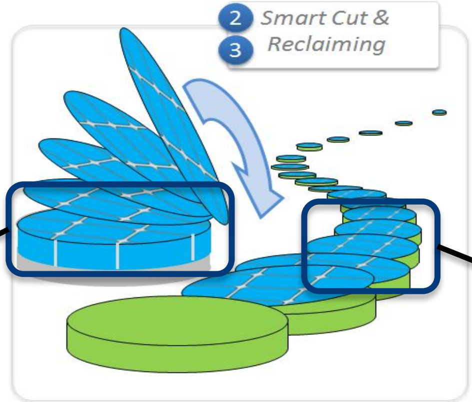
- Scaling to larger wafer diameter (200-300 mm)
- Pseudo-Donor wafer: From small InP wafers
- Handle substrate: Silicon (bulk or device wafer)
- Versatile die size and geometries
- Reuse of donor substrate



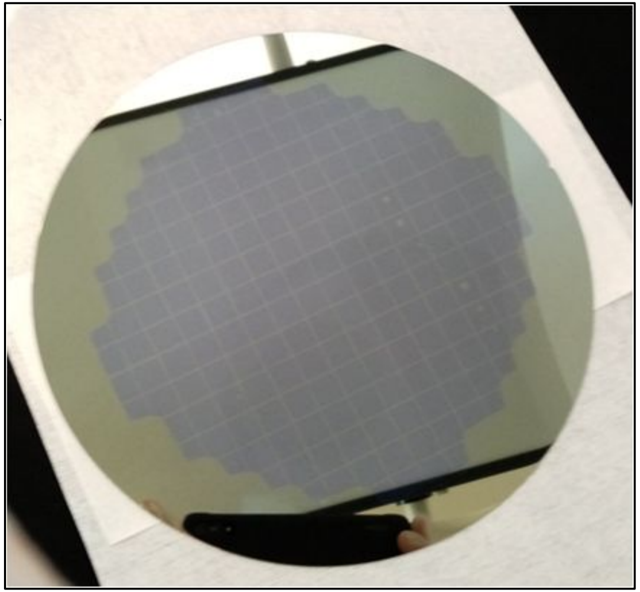
# Smart Cut™ and tiling of InP on "LARGE diameter"

## Pseudo-Donor (for reuse)



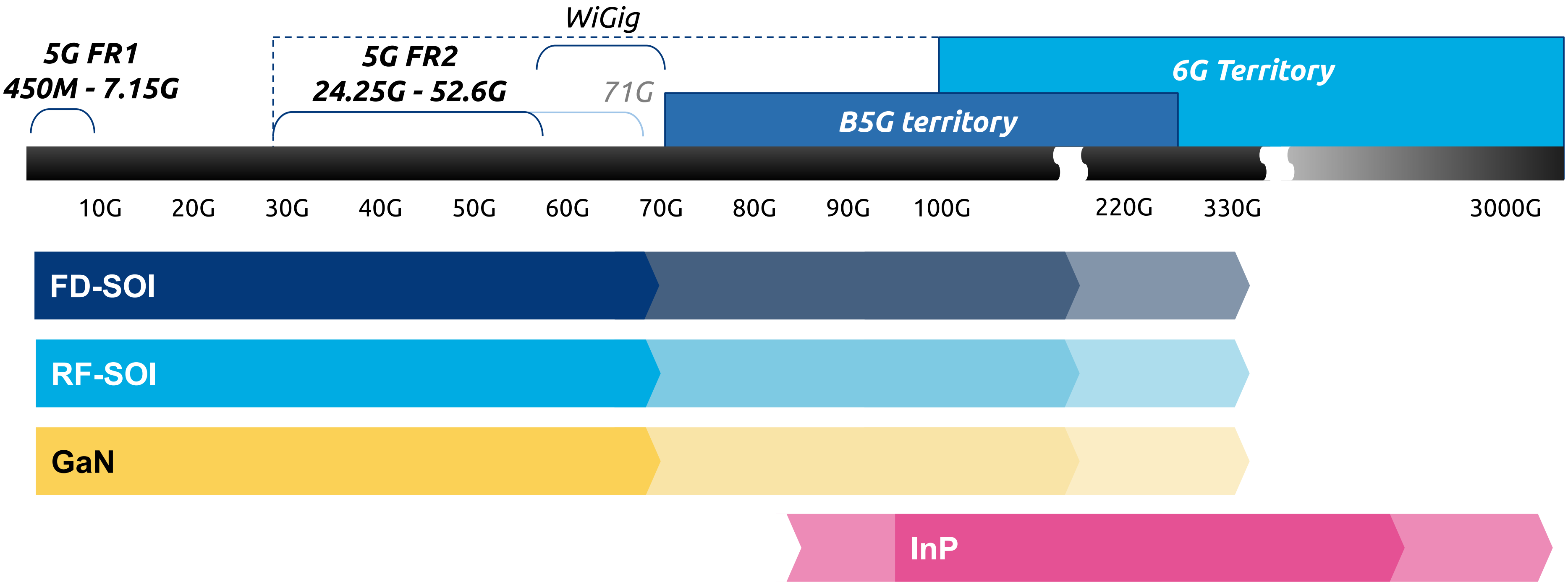



## InPOSi 200 mm (Epi ready)



## Path to 300 mm

# Takeaways




- FD-SOI, RF-SOI & GaN to be widely used for B5G
- SOITEC's InP to enable high-performance 6G applications

# Conclusions

- SOITEC's Engineered substrates already enable 5G and mmW
- FD-SOI and FD-SOI+HR SoC technology for logic/analog co-integration and efficient antenna on-chip solutions
- RF-SOI robust solution for sub-6GHz and mmW RFFE applications
- GaN solutions, GaN on (RF-)SOI, to enhance GaN adoption for handset application at mid-band mmW
- Existing, enhanced, and new substrate materials (InP) will be used for B5G and 6G

# Thank you

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# State-of-the-Art of FD-SOI technology at mmW for FEM

## PA

| | Techno | Vdd | f0 [GHz] | Gain [dB] | Psat [dBm] | P1dB [dBm] | PAE max | PAE 6dB backoff |
|---|---|---|---|---|---|---|---|---|
| Torres'18 | 28 FD | 1.98V | 31 | 21.9 to 32.6 | 17.3 to 17.9 | 15.3 to 11.6 | 24.7 to 25.5 | 11.5 to 10.4 |
| Liu'18 | 22FDX | 0.8V | 28 | 16.7 | 13.5 | 11.2 | 33.8 | 13.1 |
| Aikio'18 | 22FDX | 2.8V | 28.5 | 9.9 | 18.8 | 14.9 | 23.4 | ~14* |
| Din'18 | 28 FD | 3.15V | 24 | 9.7 | 17.9 | 16.2 | 7 | N/A |
| Mayeda'19 | 22FDX | N/A | 28 | 22.1 | 17.3 | 14 | 29.2 | ~10 |
| Zong'20 | 22FDX | 2.4V | 28 | 27 | 21.7 | 19.1 | 27.1 | 22.1 |
| Zong'21 | 22FDX | 2.4V | 28 | 26.1 | 22.5 | 21.1 | 26.2 | 19 |
| Rack'21 | 22FDX | 1.6V | 28 | 16.8 | 15.4 | 14 | 36.3 | N/A |

## LNA

| | Techno | BW [GHz] | Gain [dB] | NF [dB] (min) | NF [dB] (max) | Pdc [mW] | IIP3 [dBm] | OP1dB [dBm] |
|---|---|---|---|---|---|---|---|---|
| Gao'19 | 22FDX | 24-43 | 23<br>18.2 | 3.7<br>4.3 | 3.1<br>4.3 | 20.5<br>12.1 | -16/-19<br>30/40 GHz | ~-5/~-5<br>30/40 GHz |
| Rack'21 | 22FDX | 36.7-49.5 | 19.8 | 2.7* | 2.4* | 20 | | 3.9 |

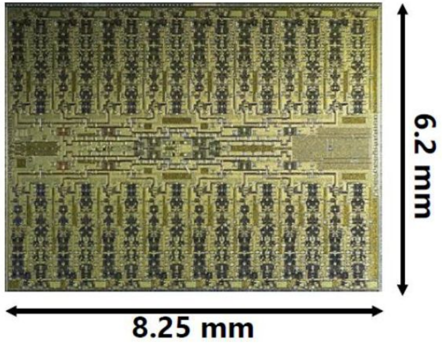
## SPDT SWITCH

| | Techno | Topology | Freq [GHz] | Ins. Loss [dB] | Isolat. [dB] | P1dB [dBm] | IIP3 [dBm] | Area [$10^{-3}$ $mm^2$] |
|---|---|---|---|---|---|---|---|---|
| Rack'21 | 22FDX | Series-shunt | DC-80 | 2.1 / 2.6<br>60/80 GHz | 25/21<br>60/80 GHz | 19.9*<br>60GHz | 33.6*<br>60GHz | 14 |

# RF-SOI solution for 28GHz phase-array beam formers FEM

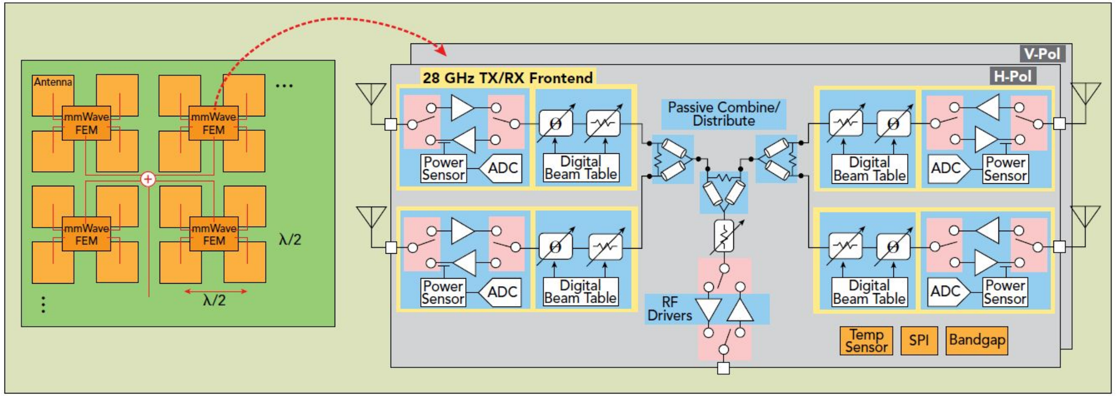
- RF-SOI provides high-level of digital/analog integration
  - required for bias/gain/phase control
  - and available memory blocks for large beam tables storing
- High-output power (>20 dBm) and gain (>30 dB), as well as breakdown voltage
- Fast and highly linear RF switches (best-in-class)
- Technology of choice for fixed-wireless CPEs and mobile infrastructure in urban environments

***28GHz 16 channel beamformer on 45 nm SOI CMOS***




***Ref: Khalil et al, ISSCC'21***

***Diagram of large-scale mmW phased array using 2x2 dual-pol. beamforming FEM***




*Source: MixComm*

# Disclaimer - non confidential