# ANTENNA-IN-PACKAGE CONCEPT FOR MMWAVE FRONT-END APPLICATIONS

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# Outline

- Challenges and Advantages of using mmWave Spectrum
- Package concept, substrate stack-up
- Material characterization
- Design of module and components
- Fabrication
- Measurement

# Challenges and Advantages when using mmWave / THz Spectrum

- Bandwidth → Data rate $C = BW \log_2(1 + SNR)$
- High path loss

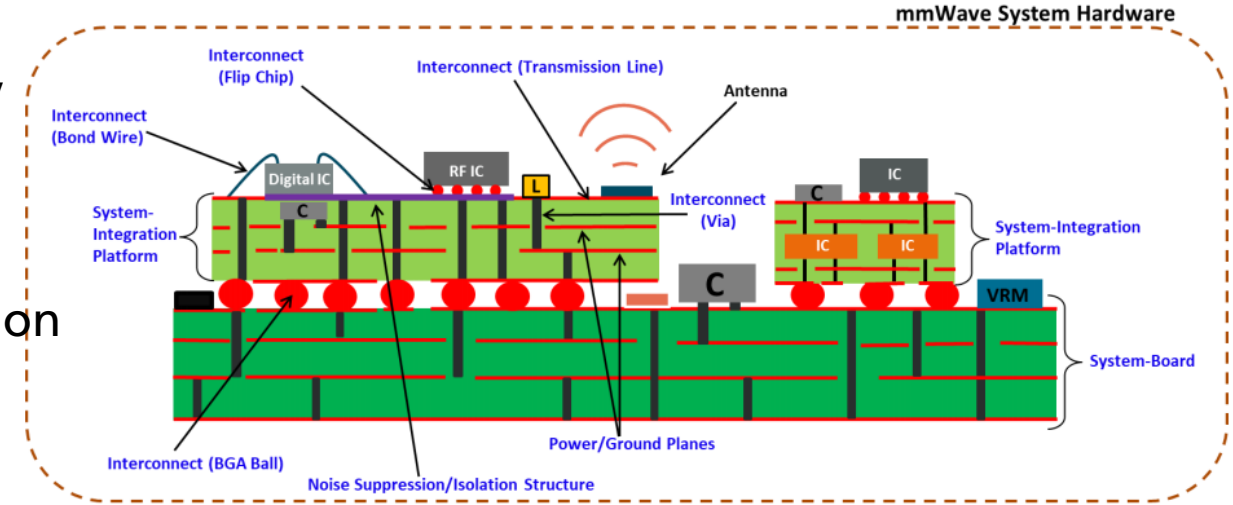
| Frequency | 3.5 GHz (n78) | 39 GHz (n260) | 140 GHz | 300 GHz |
|---|---|---|---|---|
| Free Space Path Loss (300 m) | 93 dB | 114 dB (+21) | 125 dB (+ 32) | 132 dB (+ 39) |

- Additional loss due to atmospheric (e.g. rain) and blockage (e.g. cars)
- Approach: mmWave and Beamforming using heterogeneous integration


3

# Requirements for mmWave / THz Pacakging and Antenna Integration

- Cost
- Performance / Functionality
  - Fabrication of high gain antennas $G \sim D\ e_{Subst}\ e_{Cond} e_{Match}$
  - Intry-system EMC
  - Signal/Power Integrity
  - High Q Passives
- Functional Scablability
- Heterogeneous Integration
- Miniaturization







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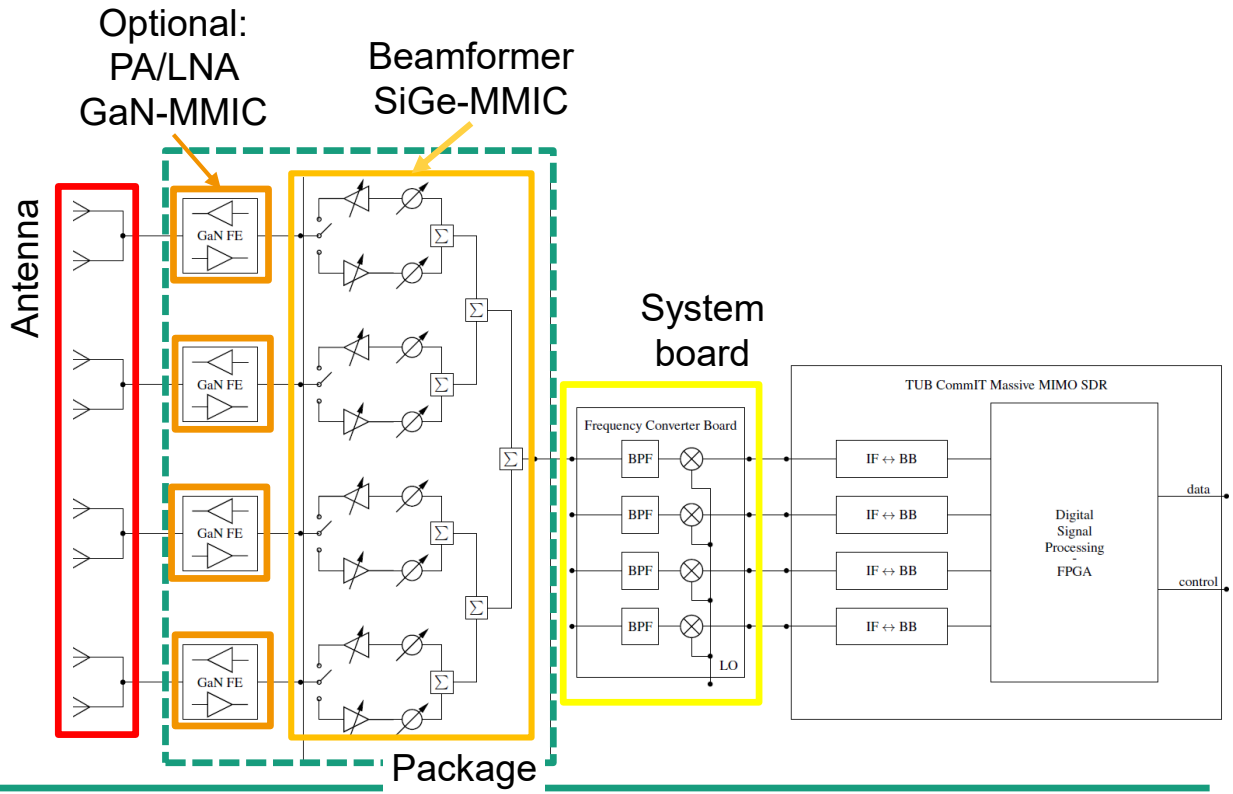
# Block Diagram

- Hybrid Beamforming demonstration system for 5G base stations
- Antenna-in package RF front-end
- Integration of
  - GaN PA/LNA
  - SiGe beamforming MMICs





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# Package Concept

- PCB Embedding Antenna-in-Package module
- SiGe Beamforming IC 39 GHz + decoupling capacitors
- 6 metal layers
- Bottom layer with LGA Interface

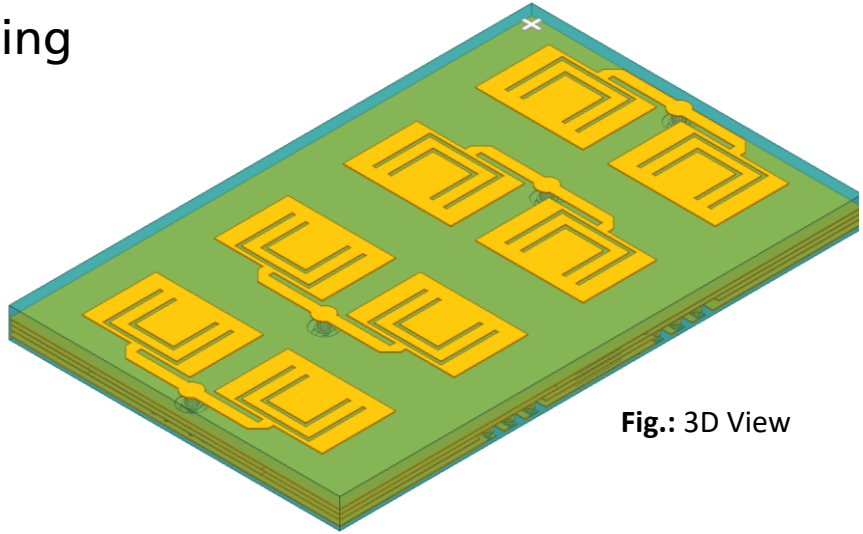
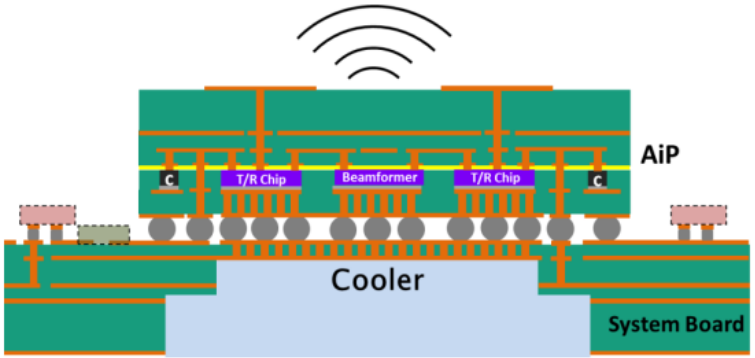


**Fig.:** 3D View




European Patent Nr. EP3346548B1; US20180191062A1

**Fig.:** Concept of SERNA module





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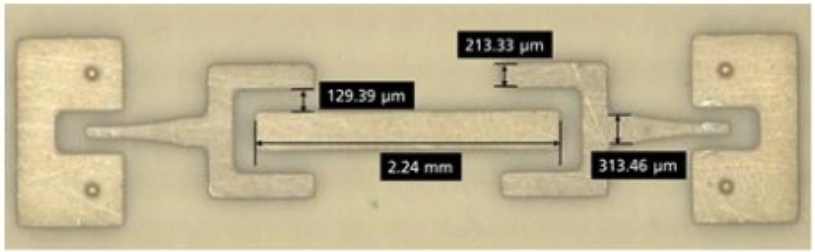
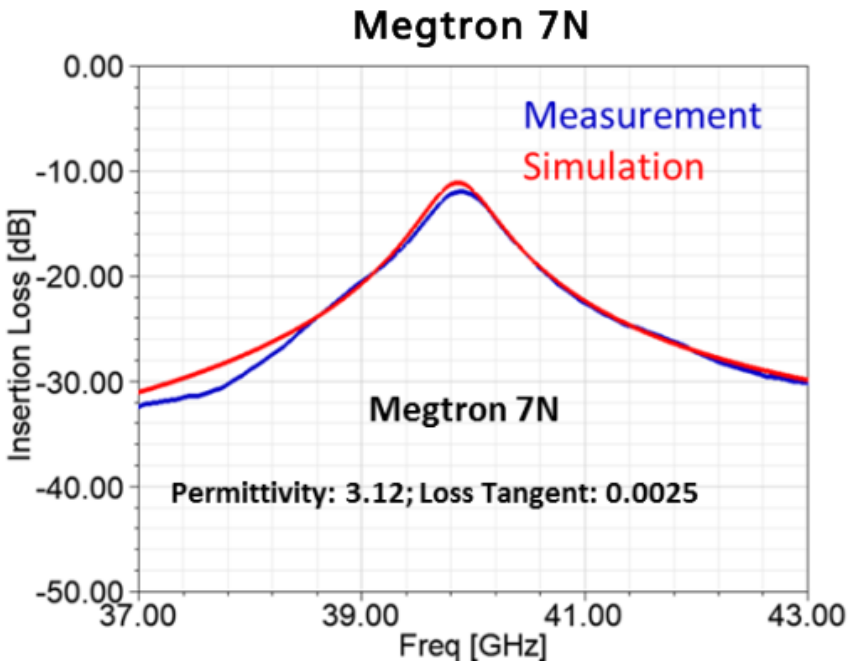
# Dielectric Material Characterization

- Dieelectric material characterization using planar resonators




Fabricated planar resonator for measuring relative dielectric constant and loss tangent of Megtron 7N substrate





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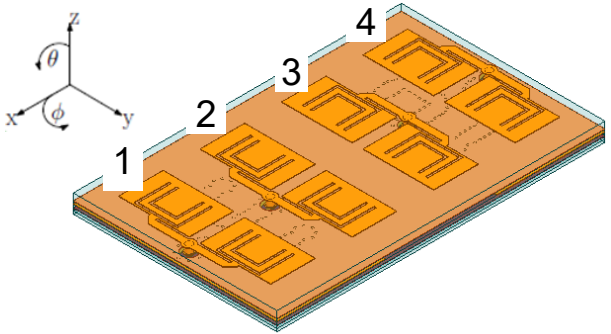
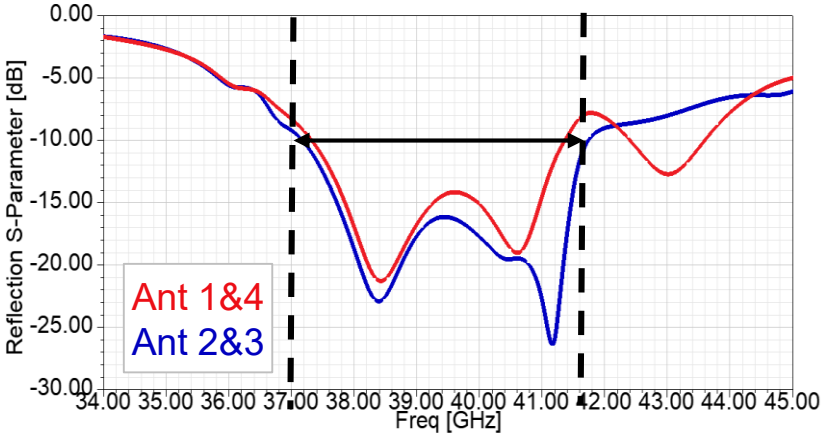
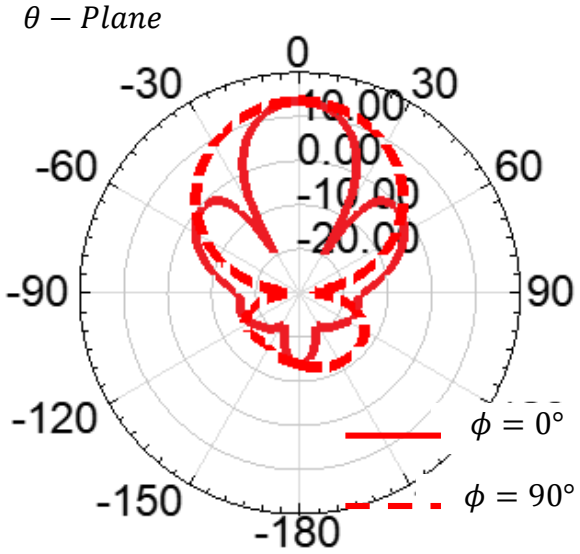
# Package Component Design - Antennas




- Antenna properties
- -10 dB bandwidth
  - Antenna 1&4: 4 GHz (37.3-41.3 GHz)
  - Antenna 2&3: 4.5 GHz (37.1-41.6 GHz)
- Realized gain (full array): 13.5dBi @ 38.5 GHz





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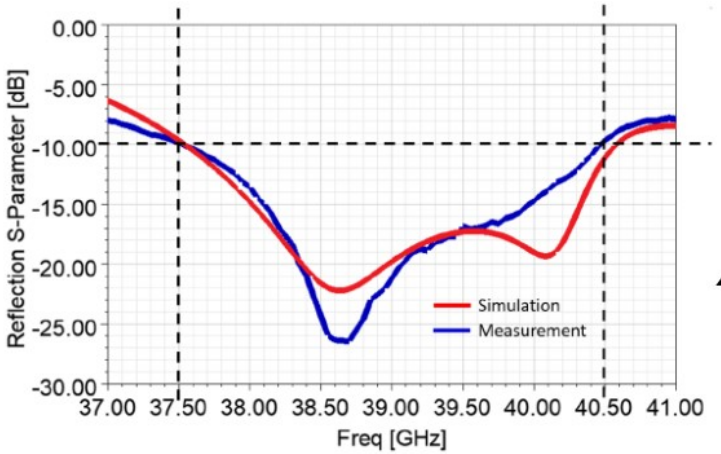
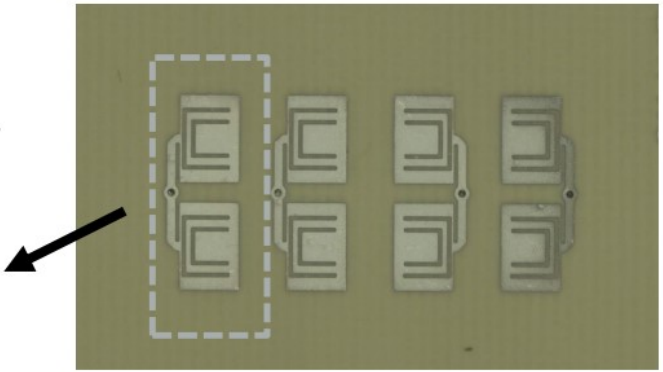
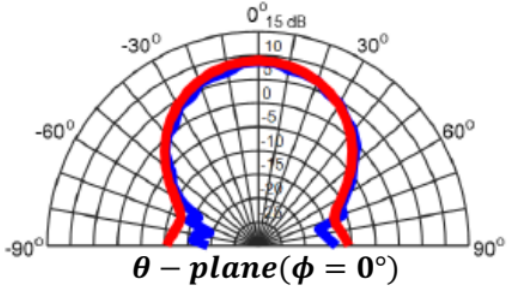
# Package Component Design Validation – Antennas



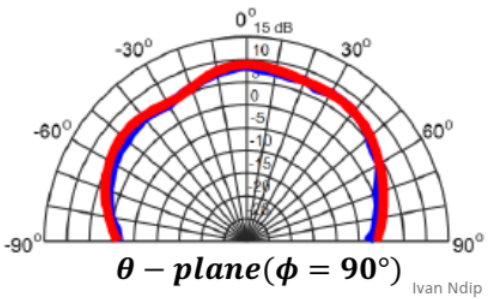



Fabricated antenna array

| Parameter | Simulation | Measurement |
|---|---|---|
| Bandwidth | 3 GHz (37.5 GHz – 40.5 GHz) | 3.1 GHz (37 GHz – 40.6 GHz) |
| Peak Gain | 9 dBi | 8.8 dBi |




$\theta - plane(\phi = 0°)$




$\theta - plane(\phi = 90°)$

Ivan Ndip





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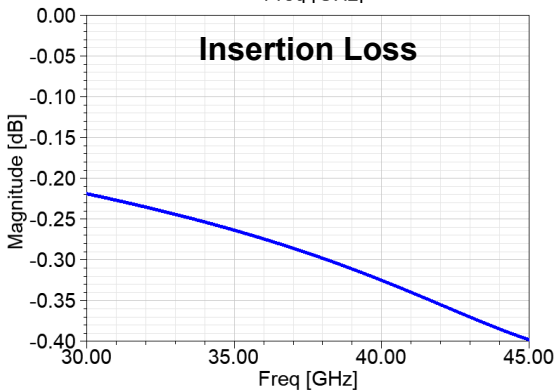
# Package Design Board-IC Interconnect

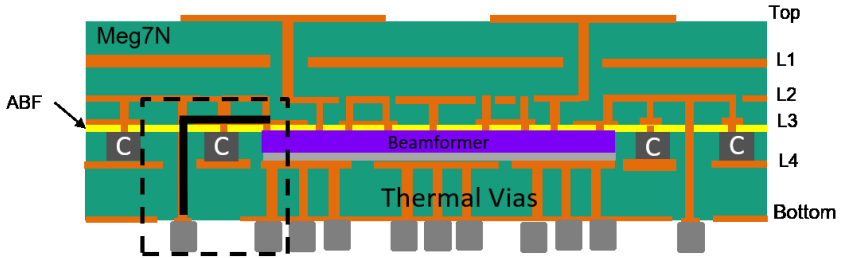




**Fig.:** Stackup of the SERENA modules

Module: GCPW
- Width: 110 µm
- Slot: 150 µm

System board: SL
- Width: 137 µm

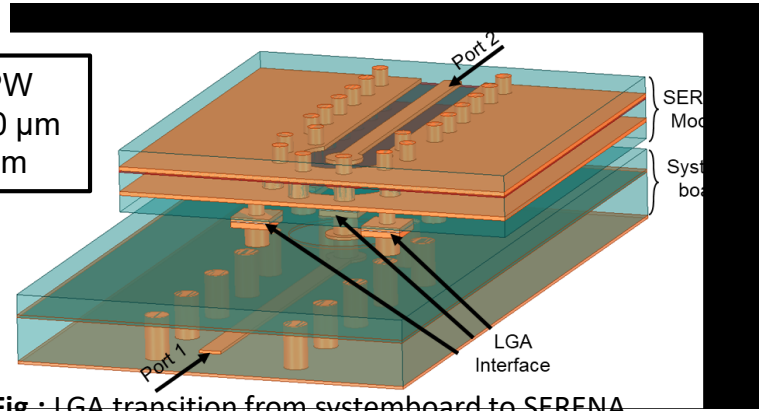



**Fig.:** LGA transition from systemboard to SERENA embedded module





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# Package Design IC-Antenna Interconnect

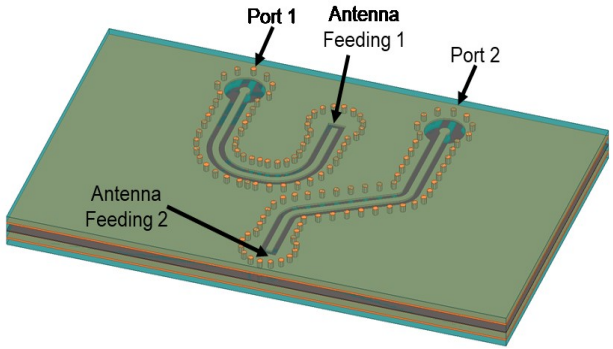
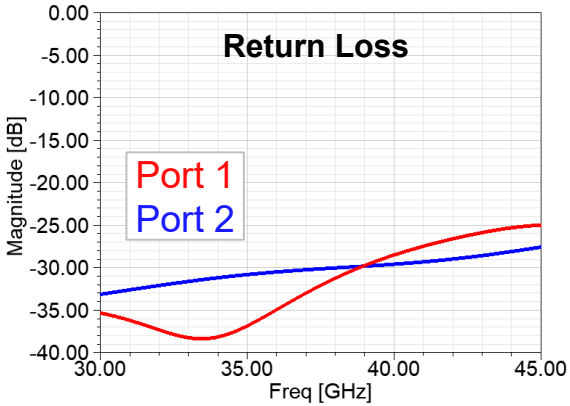


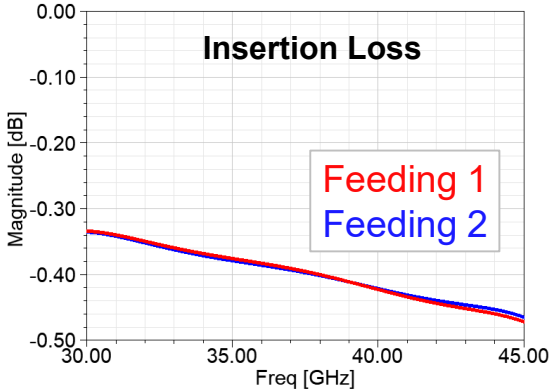

**Fig.:** Transmission lines from chip to antenna on layers L3 and L4 in the PCB Embedding module.

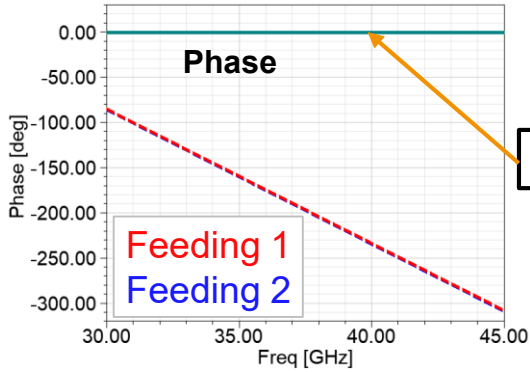
Layer 4: GCPW
- Width: 123 µm
- Slot: 100 µm

Layer 3: GCPW
- Width: 110 µm
- Slot: 150 µm

Total length: ≈ 6 mm




$\Delta_{phase} \approx 0.79$ deg





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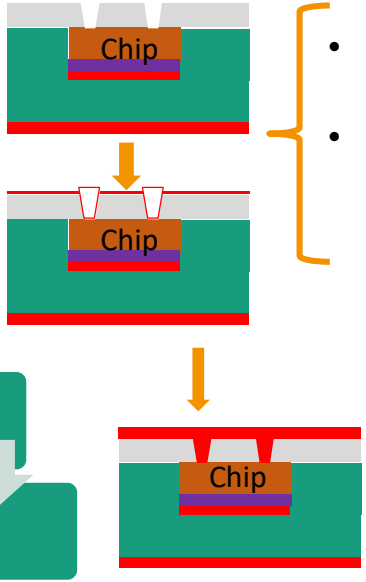
# Fabrication – Embedding Process

- Die placement (sinter glue)
- Embedding process Megtron 7N + ABF
- Laser drilling
- Sputtering process
- Electro plating




- sputtering process (plating base): 100nm TiW / 300nm Cu
- important: degassing of substrate prior to sputter process in order to ensure better Cu adhesion

electro plating: special electro plating bath with leveling characteristic (“via filling”)





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# Fabrication - Lamination

- After embedding follows the build-up of the 3 further routing layers above the embedded layer

- Main process steps for each
  - lamination
  - laser drilling
  - metallization
  - structuring
  - pre-treatment for next lamination step

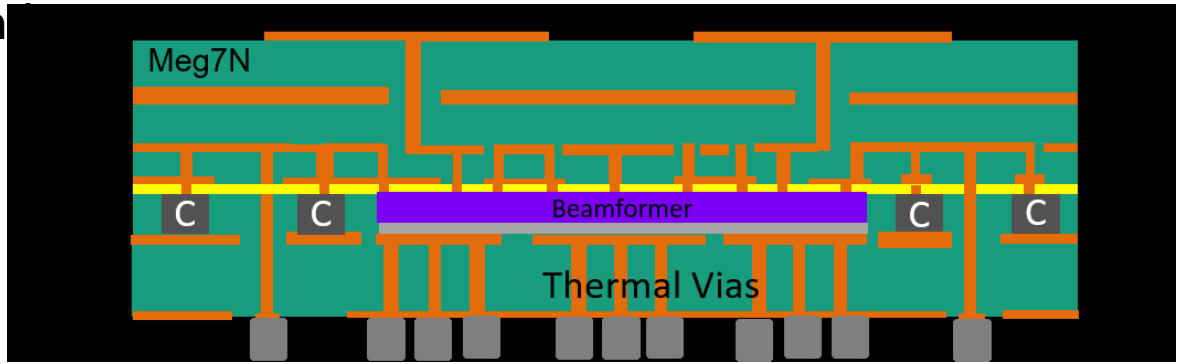


**Fig.:** Stackup of the SERENA module





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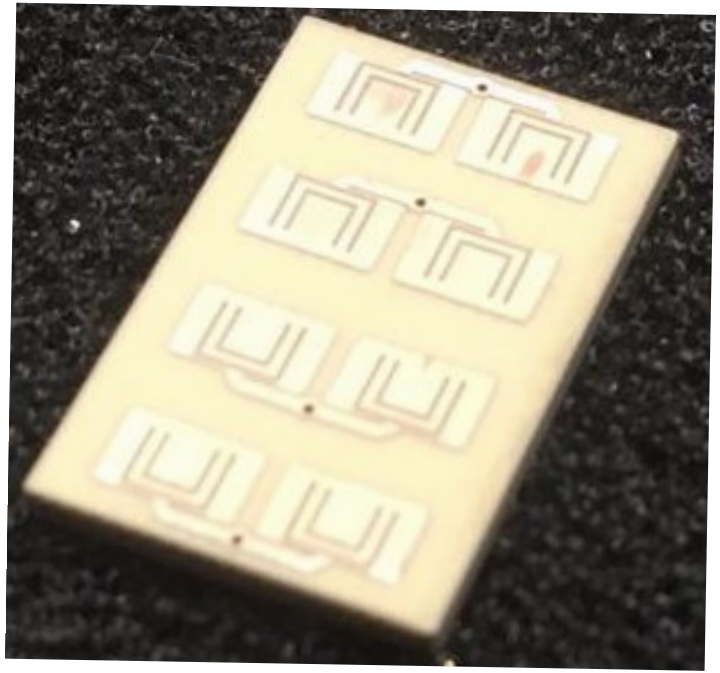
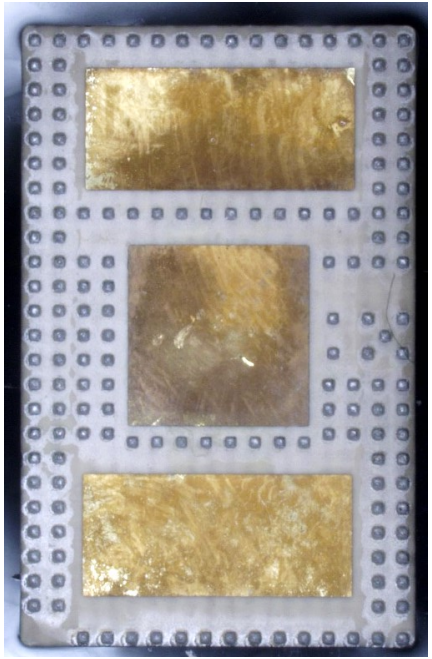
# Fabricated Module



Top: Antenna layer



Bottom: LGA layer





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# Fabricated Modules - X-ray

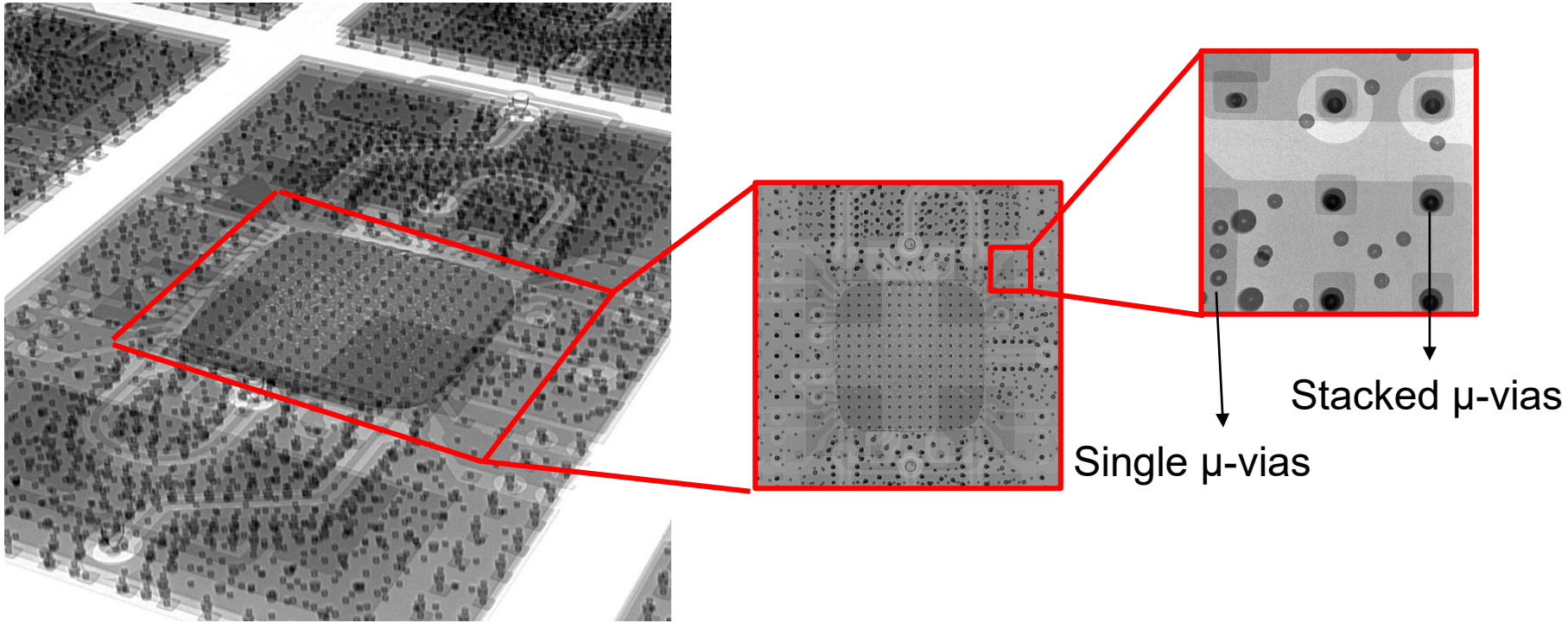


**Fig.:** X Ray - Fabricated Low power module.





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# RF Characterization Set-up

- Development of measurement set-up for verification of critical manufacturing steps using Embedding test structure with GaN PA/LNA IC
- On-wafer characterisation
  - Connected to PNA E8361A (20 – 55 GHz)
  - Tests on bare dies and assembled ICs

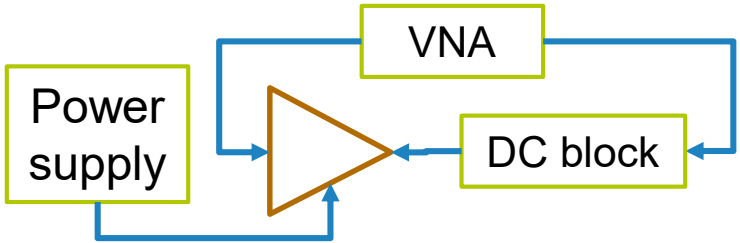
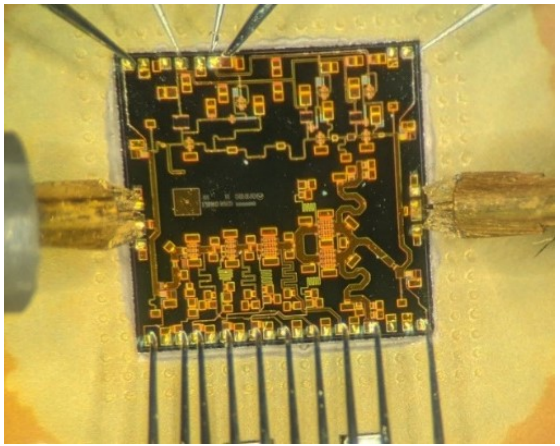



**Fig.:** Block diagramm of setup for RF measurements.





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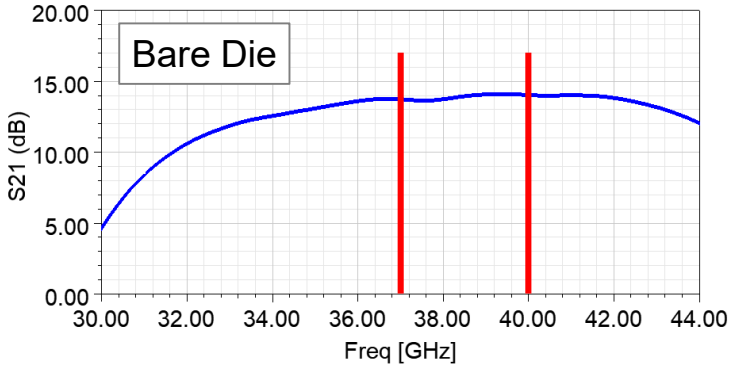
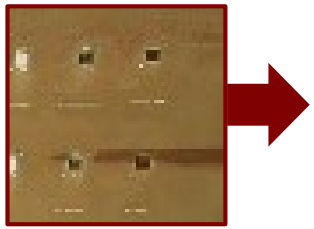
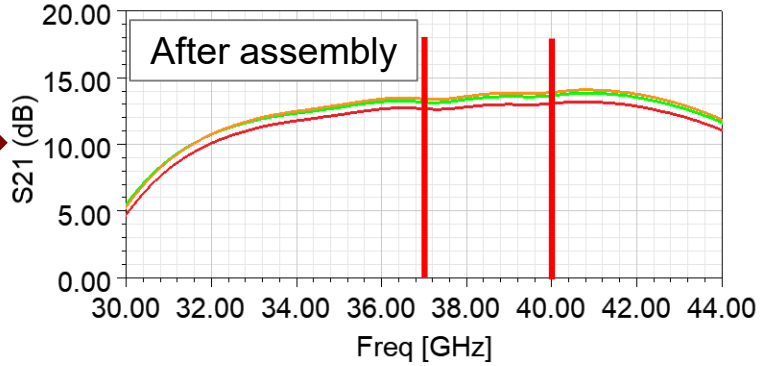
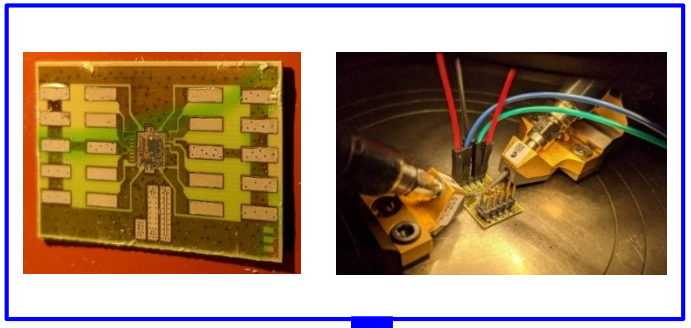
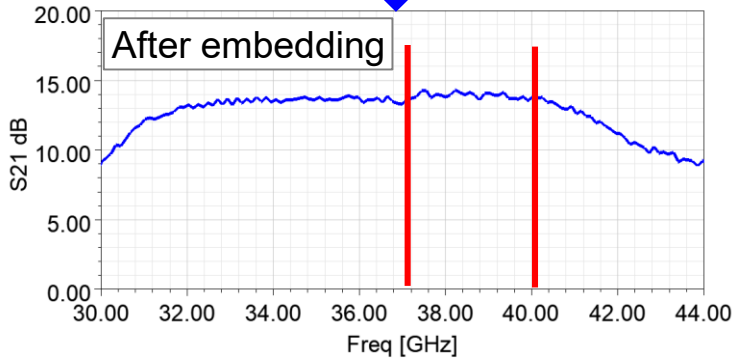
# RF Characterization – GaN LNA









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# Evaluation of Fabricated Modules

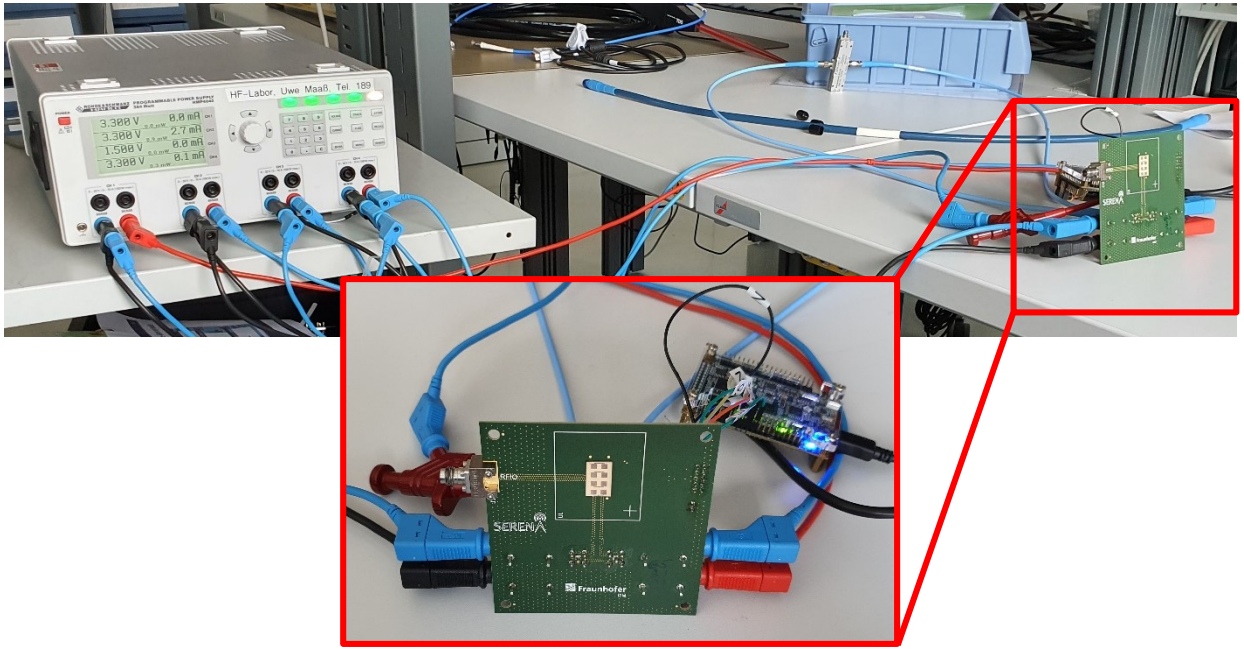


**Fig.:** Measurement set-up of module mounted on test board including SPI interface





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# Evaluation of Fabricated Modules

```
test 1/6
checking BEAM39PA status
this should print "status (0x4080): PON LOCK" after power on and "status (0x0000):" after reruning this test
**
M1B1: status (0x4080): PON LOCK
**
clearing and checking BEAM39PA status, this should print "status (0x0000):"
cleared status registers
**
M1B1: status (0x0000):
**
reseting all BEAM39PAs to be in a known state: resetting SERENA system
press enter to continue, ctrl+c to stoptest

2/6
testing register read/write of the BEAM39PA
This test uses the register PLL_CTRL_1. It tests for the default value, writes a value and reads it back.
testing BEAM39PA M1B1
  reading default value:
  * reading successful, default value correct
  writing test value
  reading test value:
  * reading successful, value correct
  writing back default value
press enter to continue, ctrl+c to stop test

3/6
testing BITE power (ADC), this should increase the current drawn at the VDD pin by probably >10mA
testing BEAM39PA M1B1
  press enter to enable the ADC
  * ADC enabled
  press enter disable the ADC
press enter to continue, ctrl+c to stoptest

4/6
testing RF power, VDDPA supply required.
Are the VDDPA pins and all VDD pins connected? Press "y" and enter for yes, just enter for no:
 ypowering up the common channel and channel 0 in RX mode, current drawing should increase by roughly 120mA.
testing BEAM39PA M1B1
  press enter to power common channel and channel 0 up
  * M1B1: powered up  press enter to power common channel and channel 0 down again
  * M1B1: powered down
press enter to continue, ctrl+c to stoptest

5/6
running MBIST tests of the BEAM39PAs, this should print "MBIST test successful"
  * M1B1: MBIST test successful
press enter to continue, ctrl+c to stoptest
```


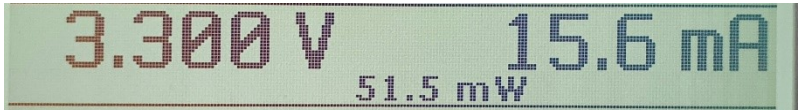



**Fig.:** Results of mounted module measurement on test board





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If you need further information, please contact the coordinator:

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