



Two-dimensional Materials in Semiconductor Pilot Lines

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RWTH Aachen University

- Large European Technical Univ.
- Public University
- 45.000 students
- Chair of Electronic Devices

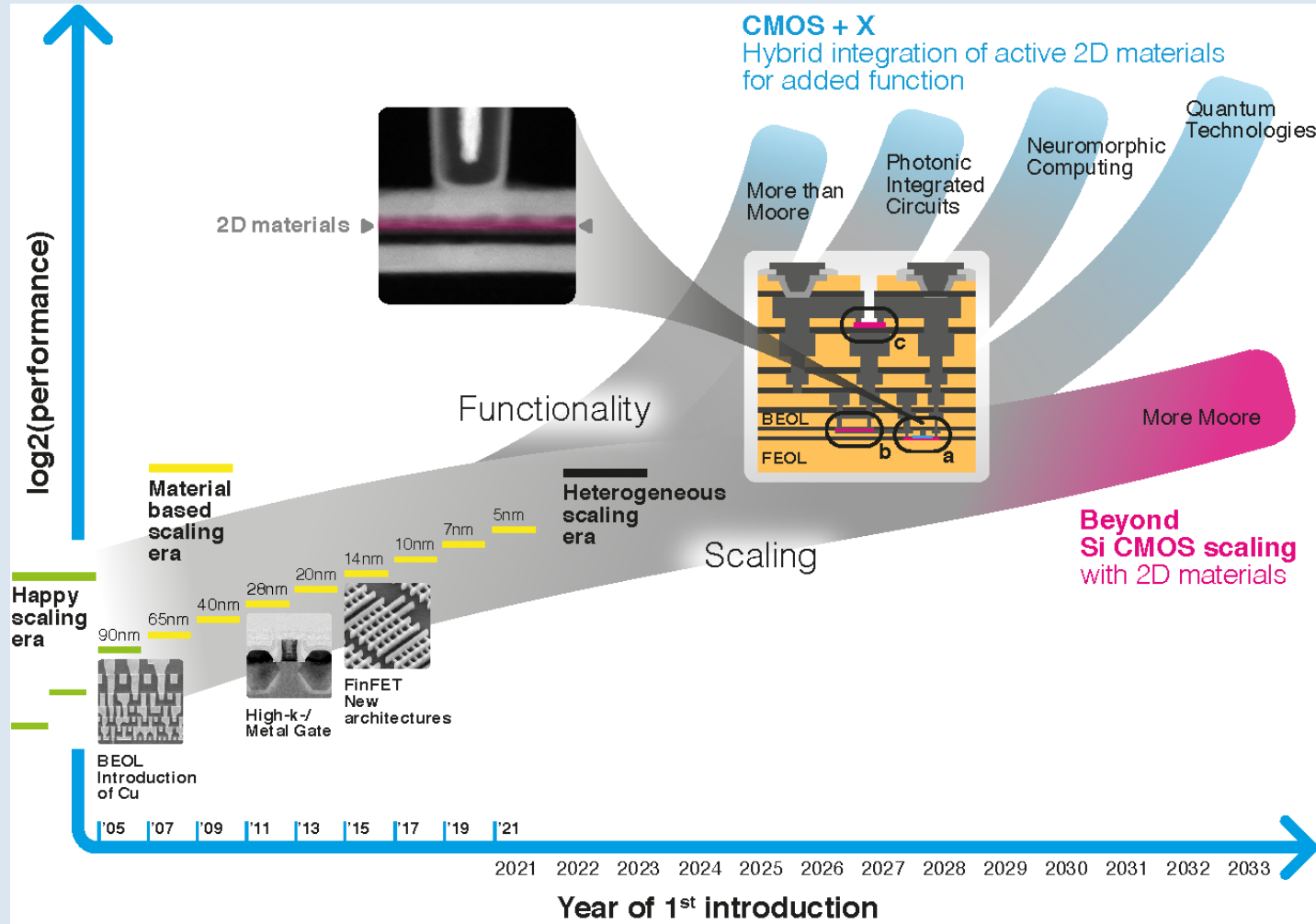


AMO GmbH

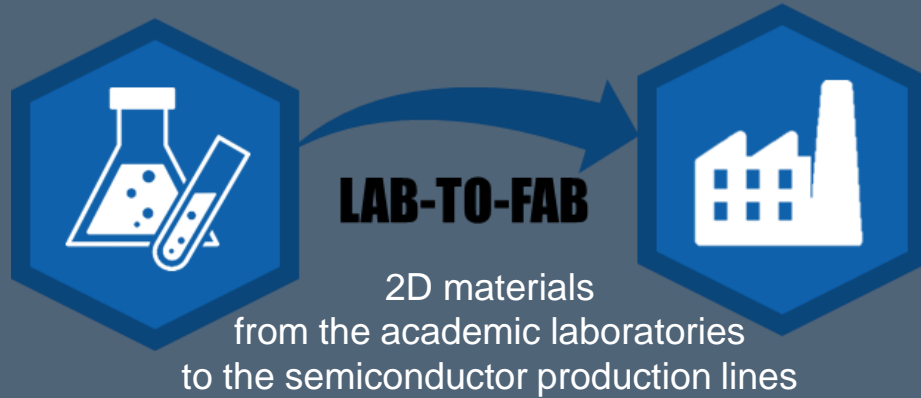
High-Tech SME / Institute (non-profit) / Research Foundry

- 400 m² clean room
- Ca. 80 staff members in 40 funded R&D projects
- Key technologies
 - Silicon technology
 - Nanofabrication & new materials integration
- Demonstrate applications
 - Nanoelectronics, Flexible Electronics
 - Nanophotonics
 - Integrated Sensors
 - Quantum Technologies
 - Neuromorphic Computing
 - Environmental Nanotechnology
- Mission: Technology Transfer
 - Project partners
 - Start Ups (Black Semiconductor, Protemics, AMOtronics)

Why 2D Materials?

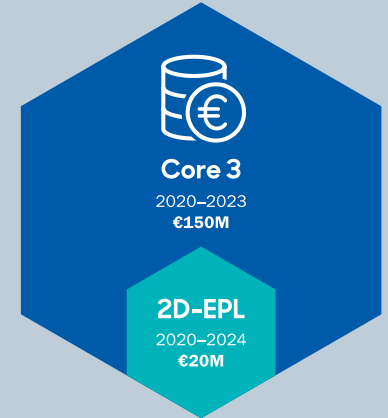


2D Experimental Pilot Line – From Lab to Fab



- Establish a European ecosystem for 2D material integration
- Make 2D Materials compatible with the standards in the industry
- Develop the critical tools, chemistry and materials
- Foundry-service with transparent access for developing new industries
- Technology transfer to commercial foundries

ULTIMATE GOAL: build demonstrators and achieve low volume production of innovative 2D technologies integrated with traditional semiconductors



- One project of the Graphene Flagship
- Started Oct 2020
- 4 years duration,
- 20 M€ funding

Approach of the 2D EPL

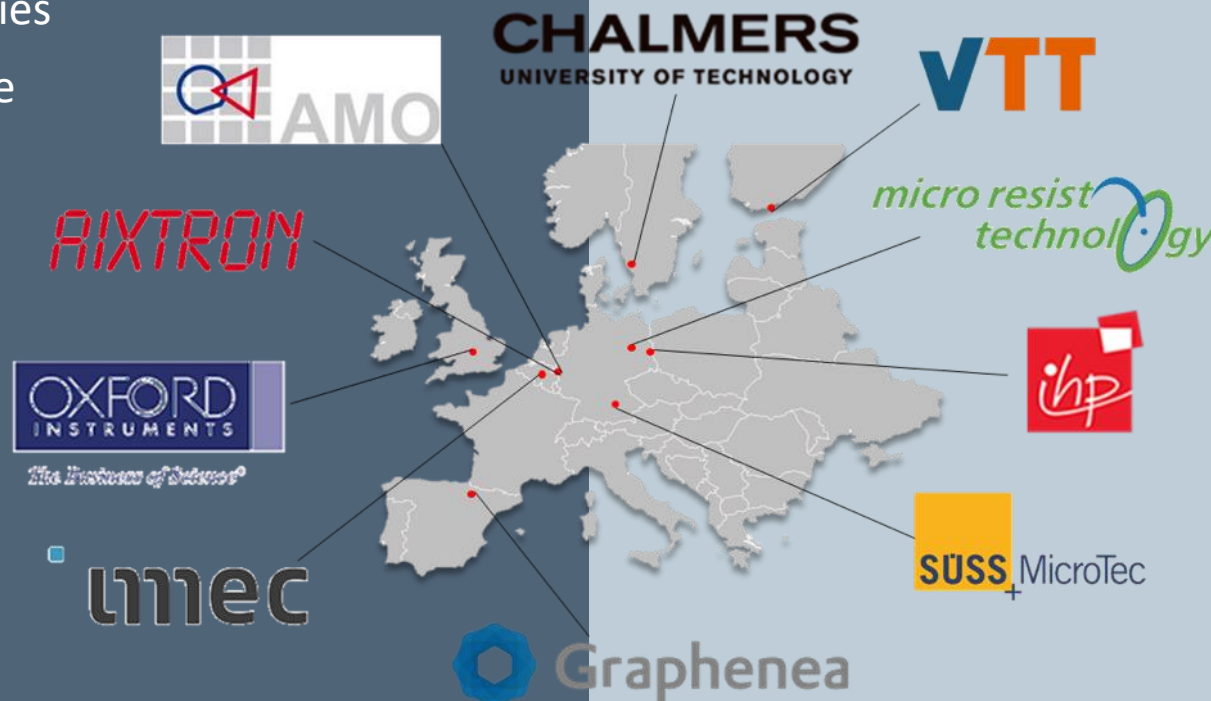
Pillar I – Prototyping from day one

- ❑ Provide processing services based on existing technologies
- ❑ Improve device performance and yield on polycrystalline CVD graphene at 200 mm platform

Pillar II – Towards generic integration platform

- ❑ Single crystalline growth of 2D materials
- ❑ Automated transfer tools for up to 300 mm
- ❑ Planarization based generic platform
- ❑ Photonics, electronics and sensor modules

11 partners all around Europe



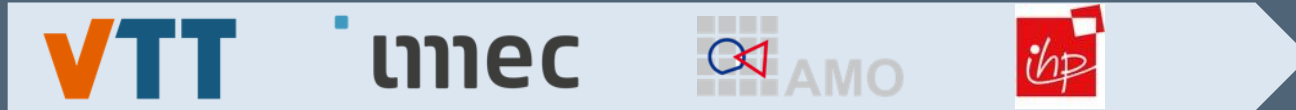
Develop the critical tools, chemistry and materials

1. Development of tools & materials



WP1 – Wafer Scale Growth
WP2 – Wafer Scale Transfer

2. Development of module & platform



WP3 – Wafer Scale Integration
WP4 – Modules for Industry

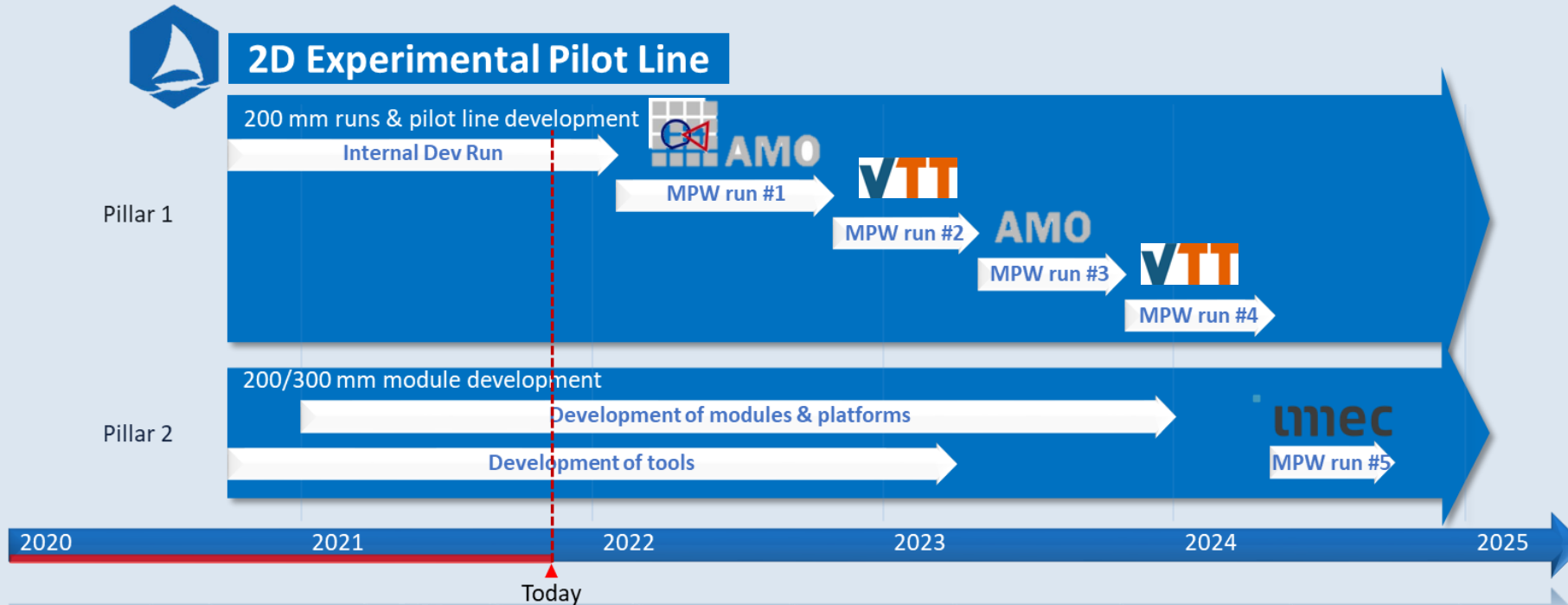
3. Multi-purpose wafer runs *(open access for testing novel ideas)*



WP5 – Multi Project Wafer



Foundry-service with transparent access for developing new industries




- Start of the project with the two pillars in parallel
- Pillar 1 just about to start the MPW run phase in parallel to the development of tools, modules and platforms
- AMO offers the first MPW run in Oct. 2022


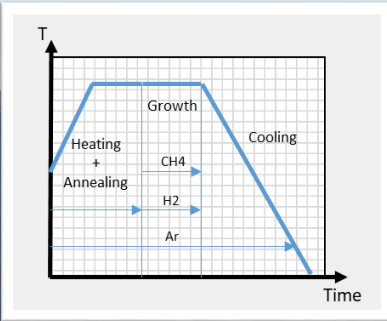
Graphene Sensors	Run 1
• Bio/Gas/Chemical sensors, Hall Sensors, Photodetectors	
Graphene Sensors	Run 2
Electronic Devices incl. Graphene Sensors	Run 3
Graphene Sensors devices on CMOS wafers	Run 4
TMDC based transistors	Run 5

The 2D Experimental Pilot Line at AMO

1. Wafer Scale Growth



200 mm Cu Foil for graphene growth

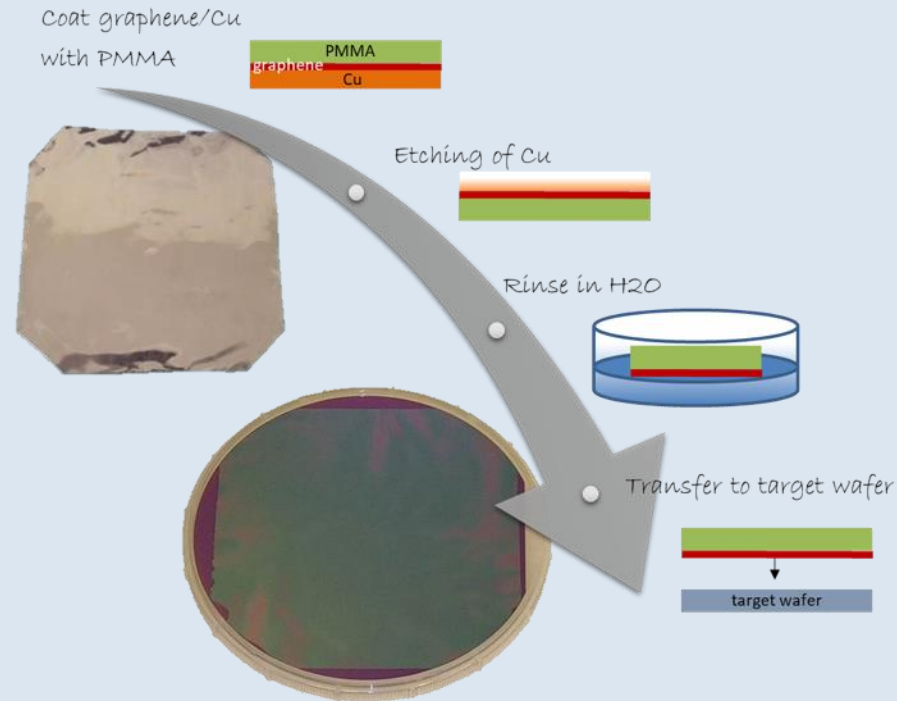



Baseline process of graphene growth on Cu Foil

- Oxford NANOFAB
- 8" compatible
- Temperature: 1200 deg.C
- Max. pressure: 4 Torr

CVD Tool used for graphene growth on 200 mm substrate size

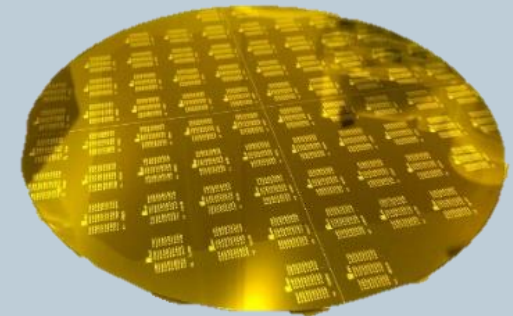
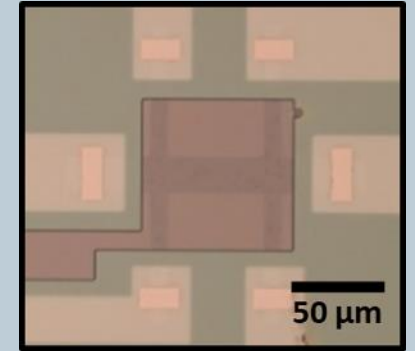
2. Wafer Scale Transfer



Nano Lett. 2009, 9, 12, 4359–4363

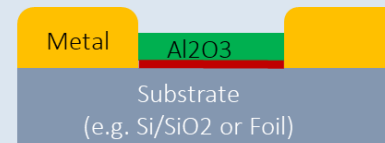
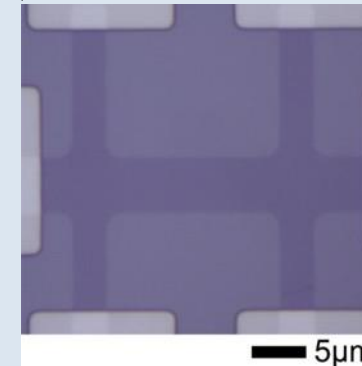
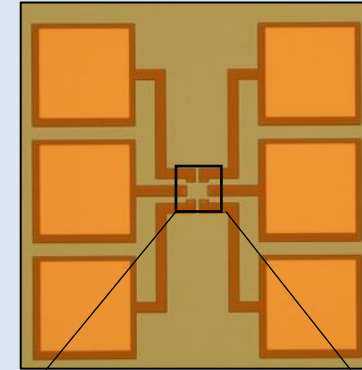
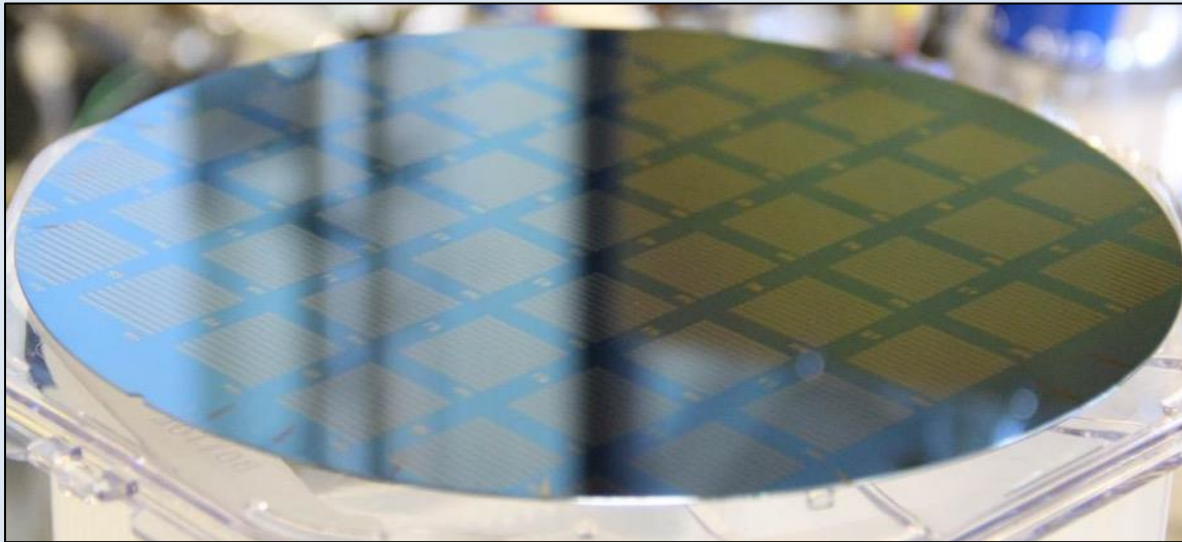
Current wet transfer process at AMO at wafer scale for 6" and 8" wafers

3. Wafer Scale Integration



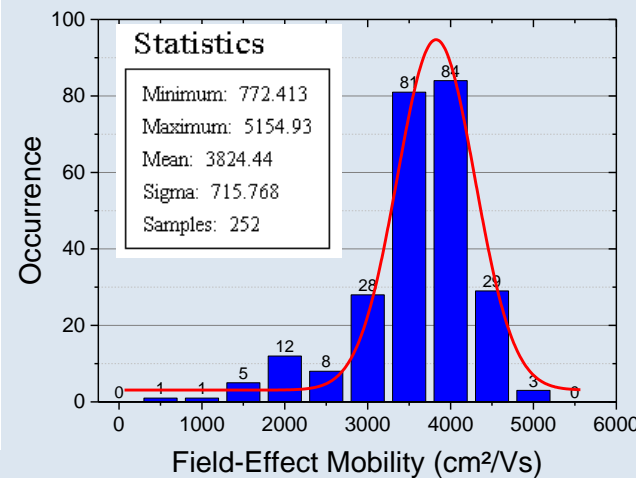
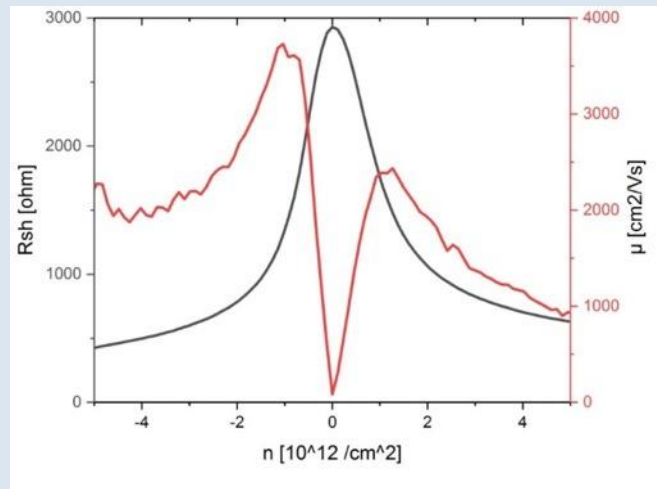
Wafer scale device fabrication with developed tools and methods

Example: Encapsulated GFETs with Global BG

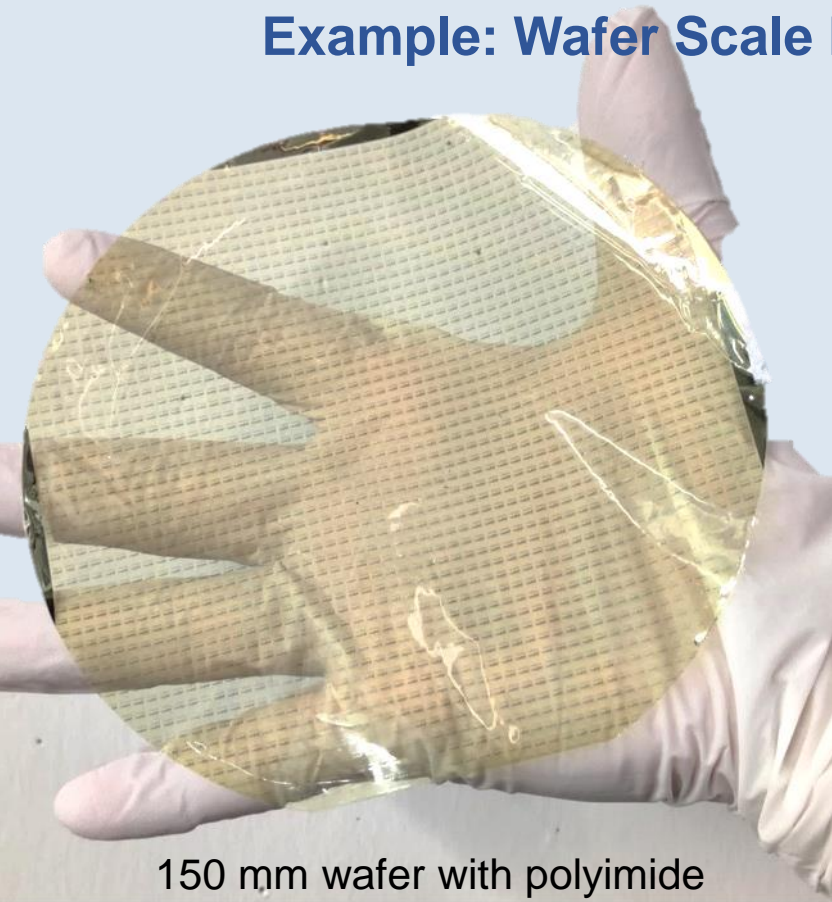


Encapsulated GFETs with global BG

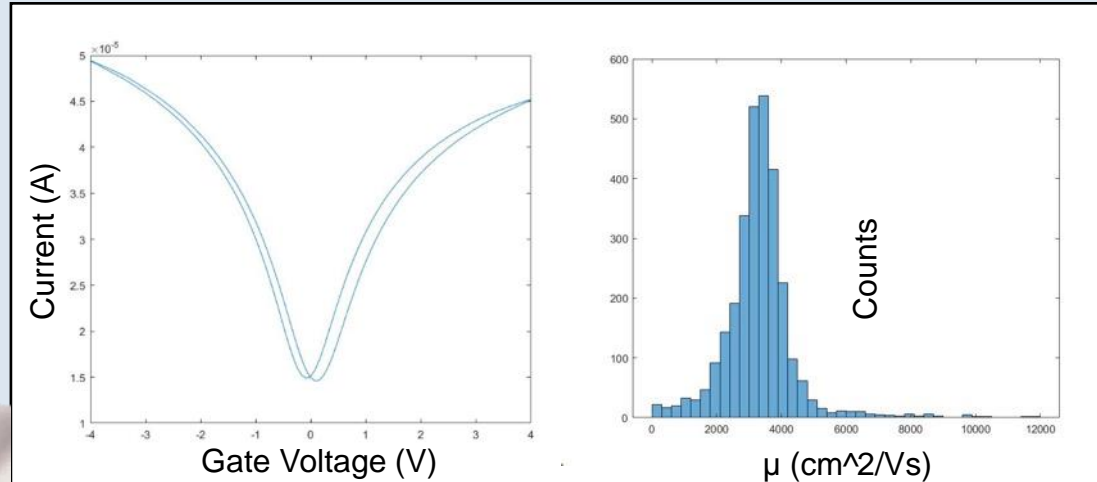
- Example of a processed 6" wafer with GFET
- 252 devices analyzed
- avg. Mobility $\mu \sim 3800 \text{ cm}^2/\text{Vs}$
- Target 2D-EPL: $\mu > 5000 \text{ Vs/cm}^2$ on 200 mm wafers with $> 80\%$ uniformity over wafer



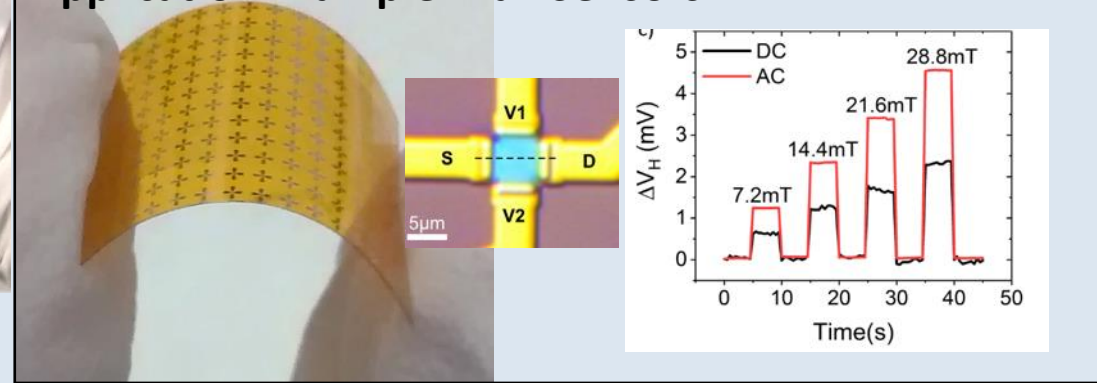
Example: Wafer Scale Process on Flexible Substrate



150 mm wafer with polyimide
 Top gate FETs as test devices
 4 point van der pauw measurement
 Average mobility: 3230 cm²/Vs



Application Example: Hall Sensors



2D EPL - MPW Run #1 @ AMO

Application

- Bio/Gas/Chemical sensors, Hall Sensors, Photodetectors

Substrate

- Material: Silicon
- Basic die size: 1 x 1 cm² (a different size can be consulted upon individual request)

Resolution

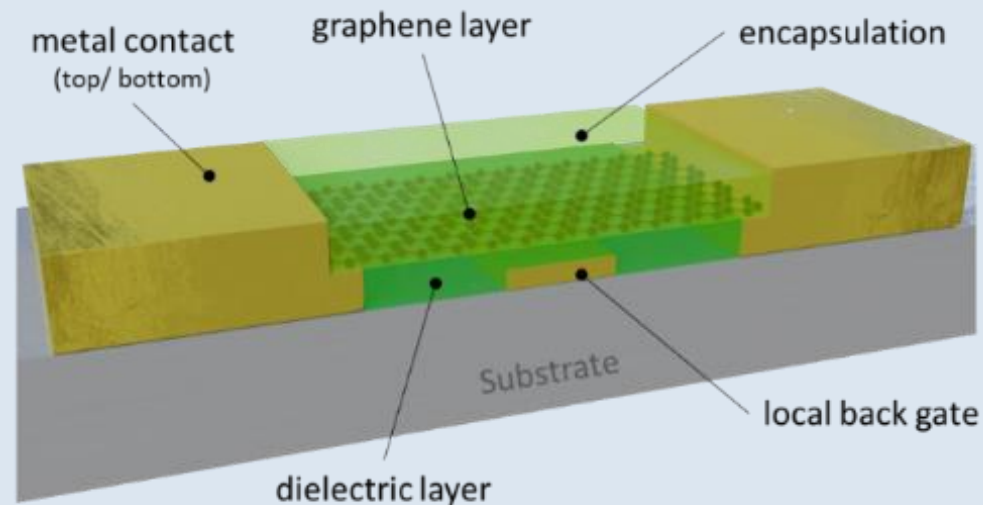
- General design rule: 5μm for in-layer critical dimension and over-layer alignment

Characterization

- Raman characterization
- Basic electrical device measurements

Baseline Process:

- Top/Bottom metal contact
- Wafer scale graphene transfer
- **Optional:** metal local or global back gate
- **Optional:** encapsulation, and via opening on top of metal pads
- **Optional:** graphene sensing area opening
- Device Library provided in PDK: Hall cross, TLM devices, 4-point measurement bar

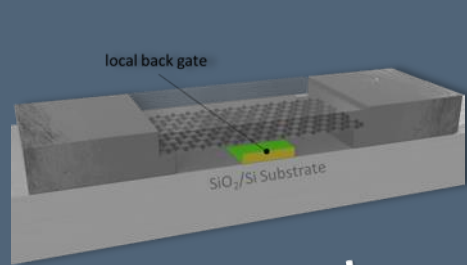
**Important Dates**

1 February 2022:
Call opens

30 June 2022:
Call closes, design freeze

2022:
MPW run

MPW Run #1 Modules

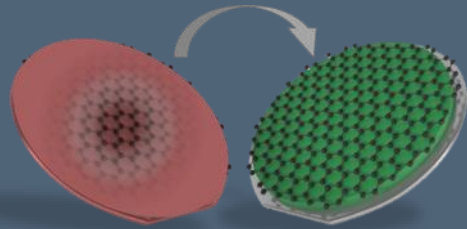


Gate Module

- **global back gate** is realised through **p-doped SiO₂/Si** substrate
- **local back gate** by 5/40 nm Ti/Pd
- **gate dielectric** by Al₂O₃ with a thickness of 75 nm grown by ALD

ongoing development

- *Local top gate*

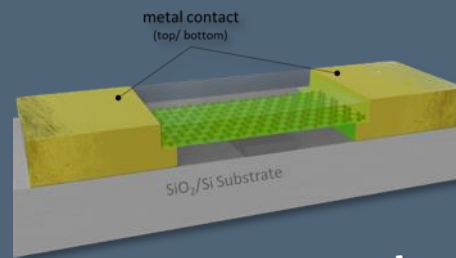


Graphene Module

- **CVD Graphene** on 200 mm x 200 mm Cu foils
- **Graphene wafer scale transfer** by semidry method or wet transfer
- **graphene patterning** by photo-lithography and reactive ion etching

Mobility: 1000 – 2500 cm²/Vs

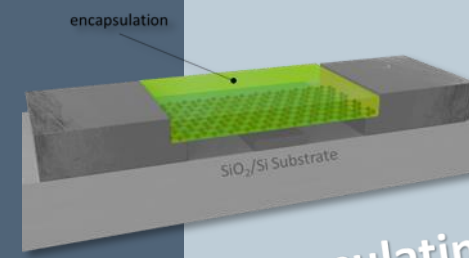
- *mobility improvement => 5000 cm²/Vs*



Graphene Contact

- **Sandwich contact** by of bottom and top Pd metal layers
- Pd layer thickness in the range of **30-50 nm**

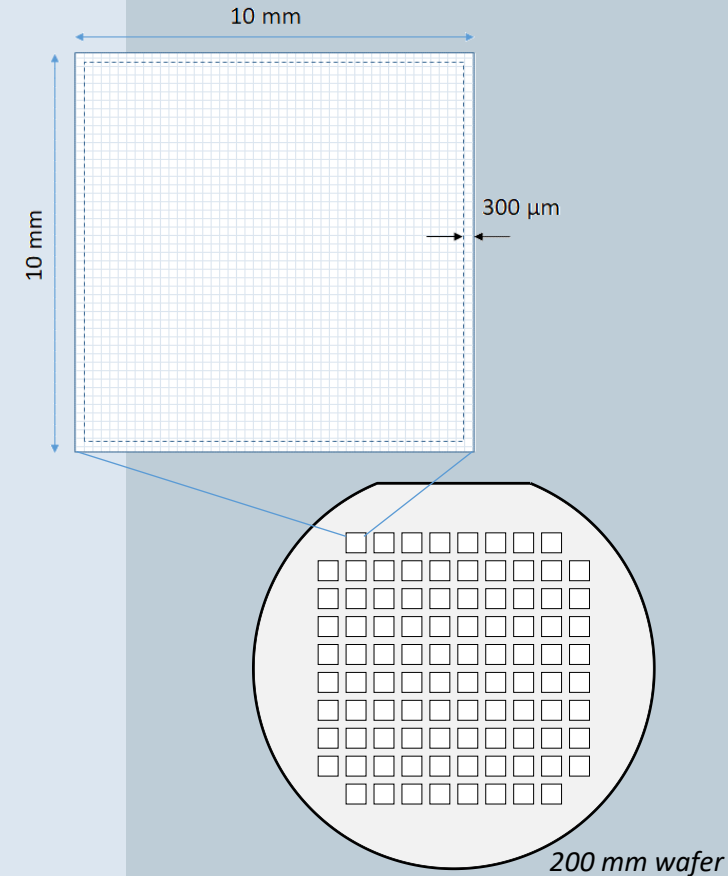
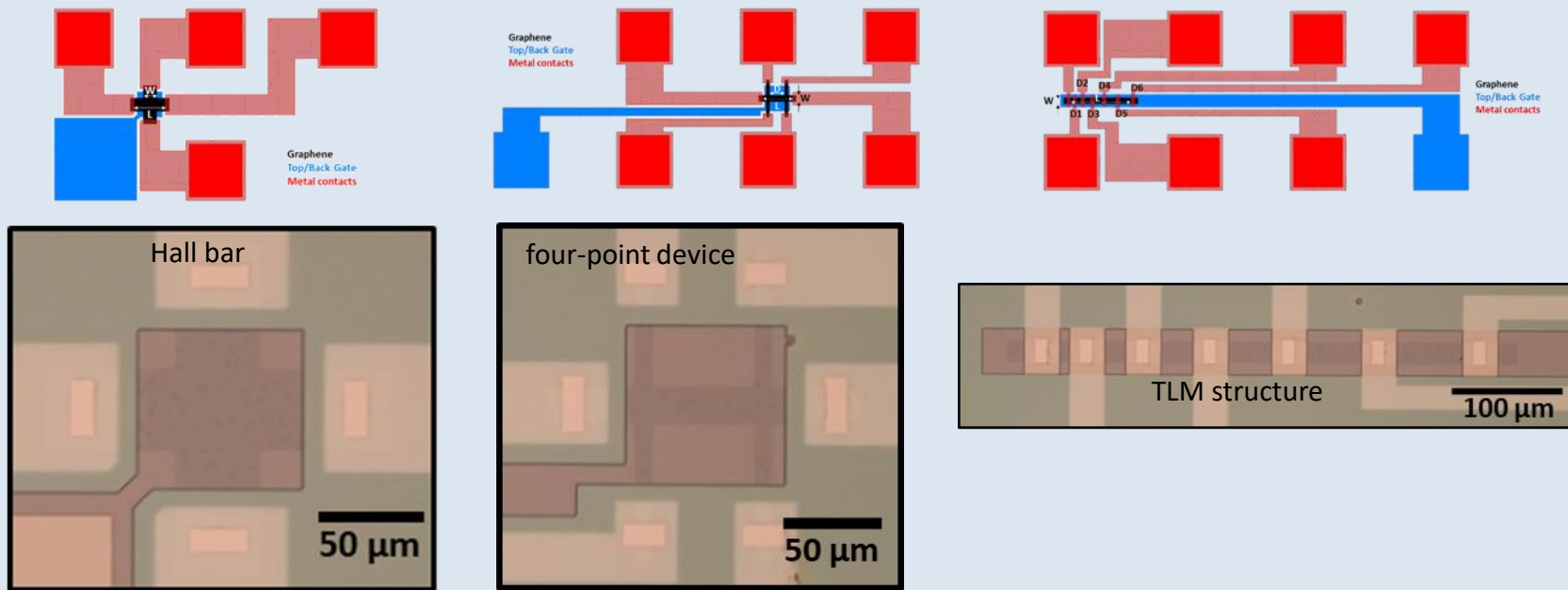
- *lower contact resistance*



Graphene Encapsulating

- Encapsulation by ALD deposition of **30-80 nm Al₂O₃** and via etching
- Encapsulation by **SU-8 coating (>7μm)** and patterning

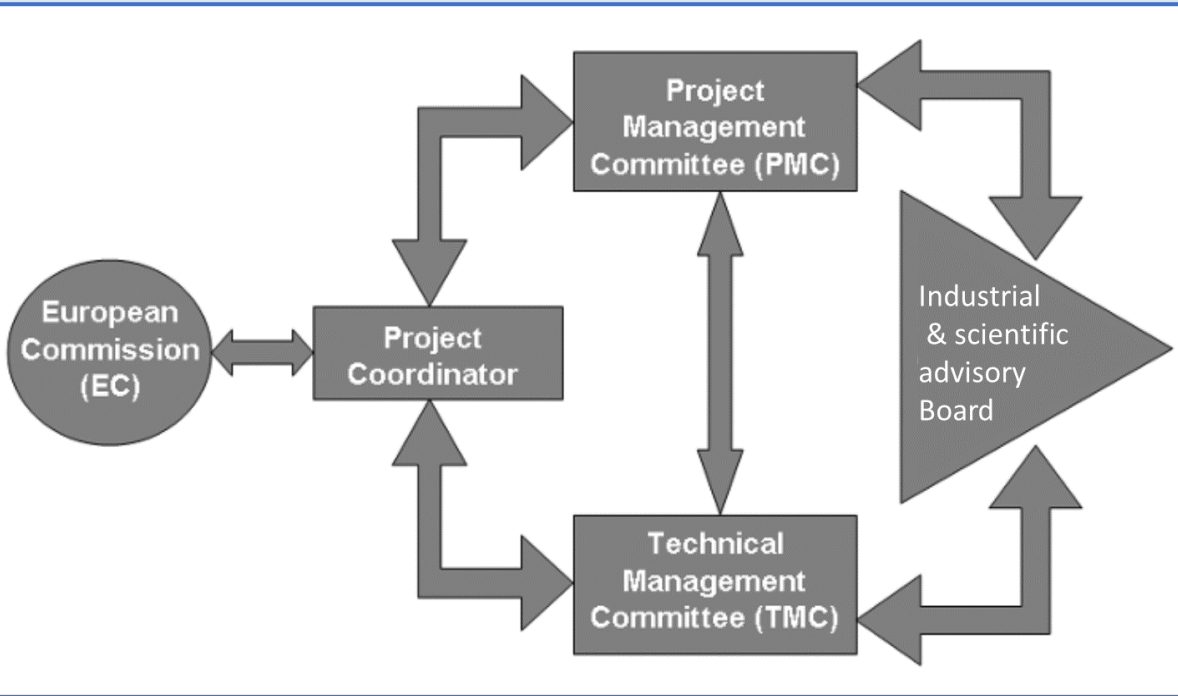
Device library and die design



- Full custom design inside 10 mm x 10 mm die size within the design rules
- Device Library available for standard reference devices available:
 - hall bar, four-point, TLM

Technology transfer to commercial foundries

Chalmers, imec, AMO,
VTT, Graphenea

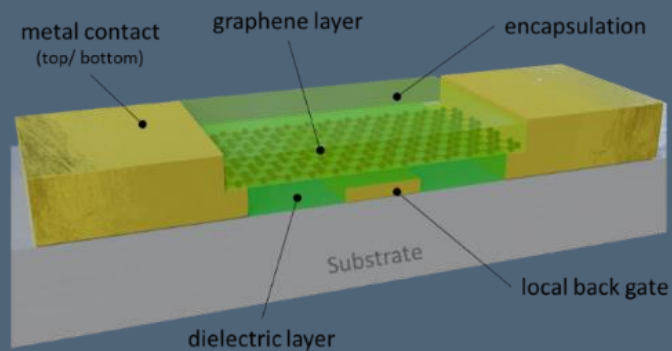


Industrial Advisory Board
X-FAB
AMS
NXP
Infineon
STMicroelectronics
Emberion
Nokia
ELMOS
Representative Flagship 1
Representative Flagship 2

➔ Semiconductor industry as Advisory Board

Summary - Establish a European ecosystem for 2D material integration

- 2D EPL Project wants to bridge the gap from lab to fab
 - ⇒ developing tools, materials, modules
 - ⇒ Providing access to the current technology for 2D Material processing
- AMO is one of the pilot line locations beside VTT and IMEC
- AMO will provide first MPW run in Oct. 2022
 - Back gated Graphene FET for applications as Bio/Gas/Chemical sensors, Hall Sensors, Photodetectors



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