SiC Power MOS technology evolution

Sustainable and efficient energy conversion in DC grids

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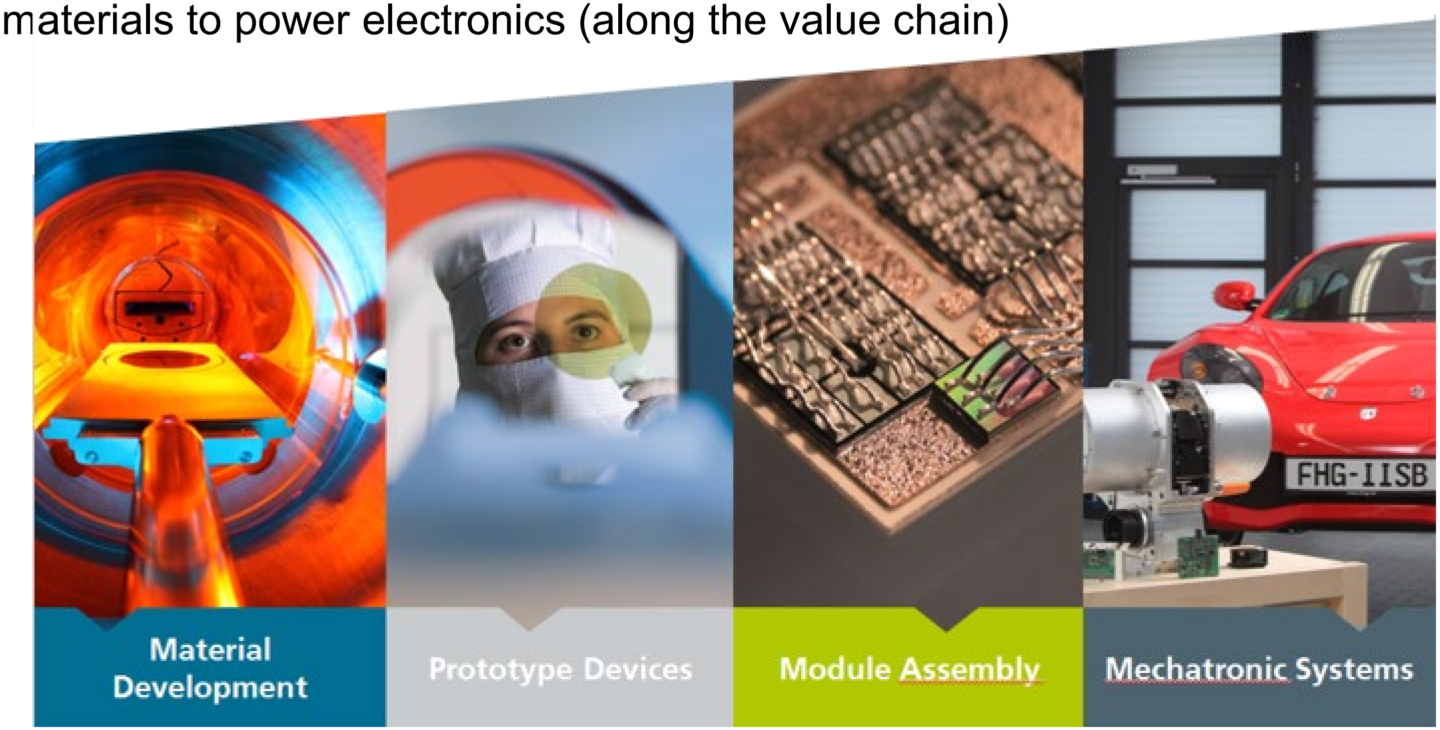
Erlangen, Germany

Fraunhofer IISB: Wide-bandgap for Power electronics

- Research and Development in Applied Science (Non-profit organization)
  - From materials to power electronics (along the value chain)



  - On the go from R&D through Prototypes to Small volume fabrication
    - R&D activities along vertically integrated value chain (internal customers!)
    - 150mm SiC CMOS technology platform with qualified process modules

Content

- Sustainability through energy efficient DC grids
  - CO_2 neutrality: Reduction and energy efficiency
  - Motivation, competition and market situation for SiC devices
  - SiC Devices: From electric vehicles to DC grids infrastructure

- Evolution of SiC Power MOS technology
  - Planar technology, wafer material and unit cell optimization
  - Trade-offs between performance, reliability and yield
  - Challenges for further advancements and moving targets

- Possible goals for further tool optimization
  - High temperature processing: Oxidation, implantation, high-temperature annealing
  - Lithography, SiC Trench etching ohmic contacts, Wafer thinning

- Opportunities and Conclusion

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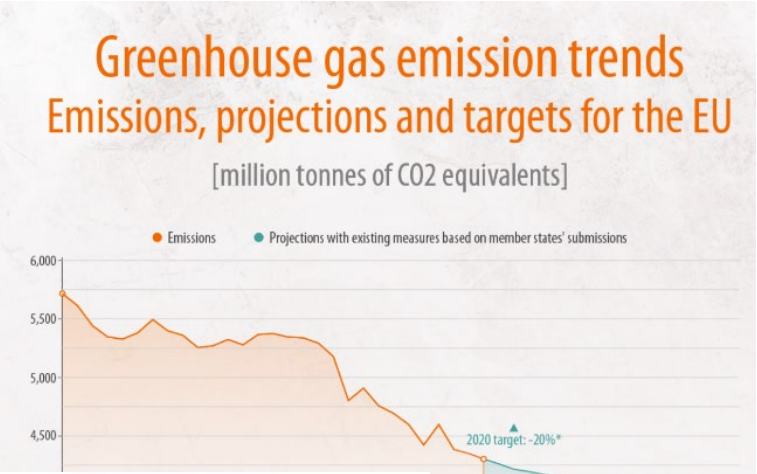
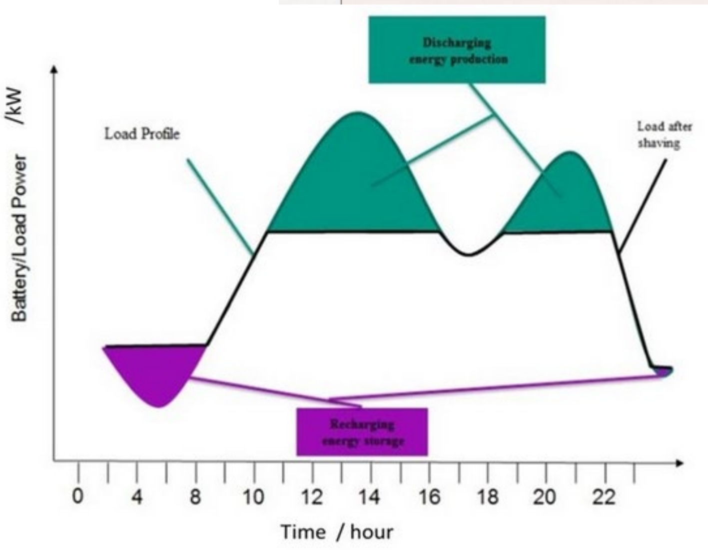
Sustainability through energy efficient DC grids

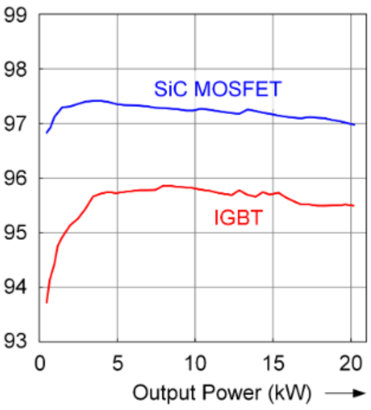
- Energy efficiency contributes to EU's CO_2 goals
  - Ecological and economical implications
    - Laws and regulations (compare Monitors)
    - Prestige and responsibility for companies

- SiC (WBG) converters offer excellent partial load properties
  - Up to 10% more efficiency compared to silicon topologies
  - Every time energy is transferred
    - Generation
    - Storage (Recuperation)
    - Consumption
  - Applicable to any source of electrical energy consumption (broad range)





Boyouk N. et al., ISGT-Europe 2018, Sarajevo



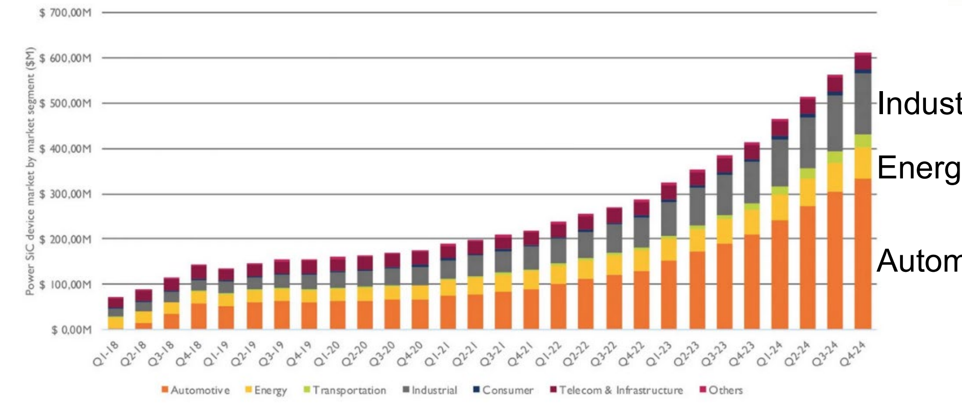
M. Nitzsche et al., PCIM 2019, Nuremberg

Sustainability through energy efficient DC grids

- Motivation, competition and market situation for SiC devices
  - Competition zone Si/SiC/GaN
    - SiC excels at 600V and above
    - High reliability demonstrated
    - Reduction of fabrication cost

Power SiC device market Forecast by segment

(Source: CS Market Monitor, Yole Développement, Q4 2019)



Industrial

Energy

Automotive

- This figure represents the estimated market for SiC devices, including both open and captive markets.
- The ramp up of automotive market in 2018 was mainly due to Tesla's adoption of SiC in its main inverter.
- Similar to automotive application, other applications such as industrial, energy and transportation are expected to grow.

YOLE Développement

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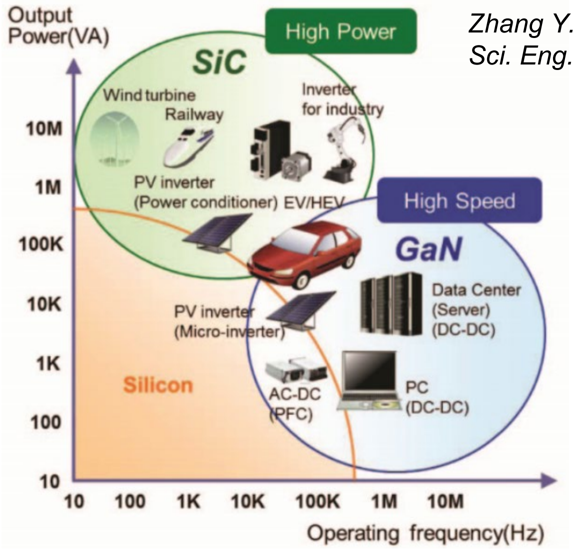
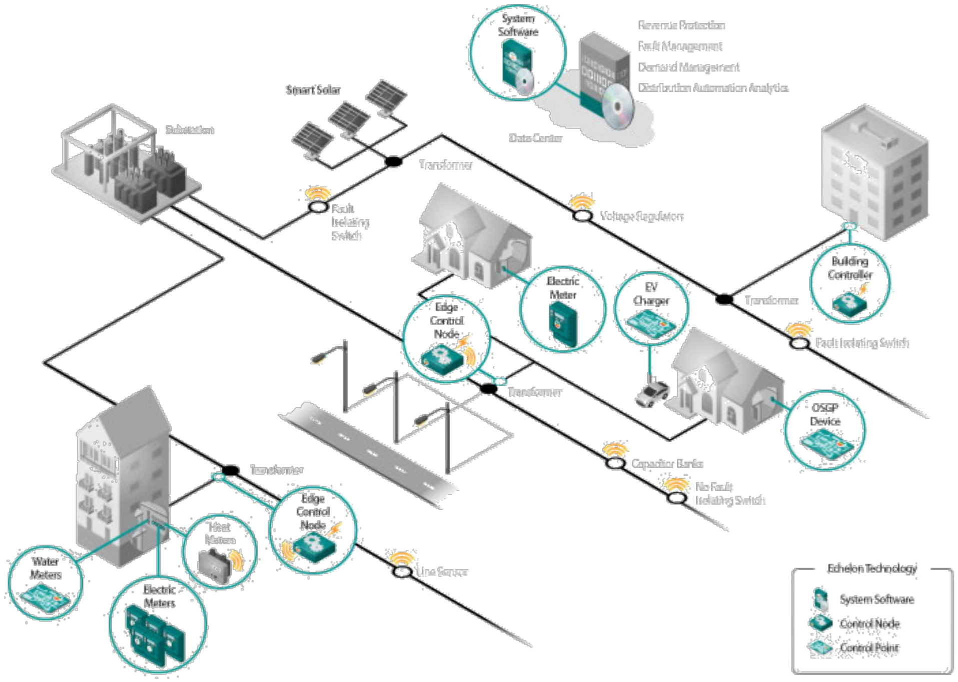


Zhang Y., Mater. Sci. Eng. ***738*** *012004*

- Power SiC market trends
  - Ramp-up is imminent
    - Tesla and Toyota kicked it off
    - OEMs are following now
  - Increase in Fab capacity
    - Fab extensions (150/200mm) & Pure-play foundries
    - “Crazy China“

Sustainability through energy efficient DC grids

- Reduction of transmission losses using SiC-based switch-mode power supplies
  - Automotive traction inverters and converters are paving the way…
  - Broad range of generation and consumption for DC grids
    - PV and Wind Power
    - Electrical storage
    - EV Charging infrastructure
    - Manufacturing tools / factories (regulated motors)
    - H2 generation (hydrolysis)
    - Lighting



  - Usually partial load conditions
    - Peak loads are the exception

      → Converter designed for peaks
    - Load shifting or Peak shaving?

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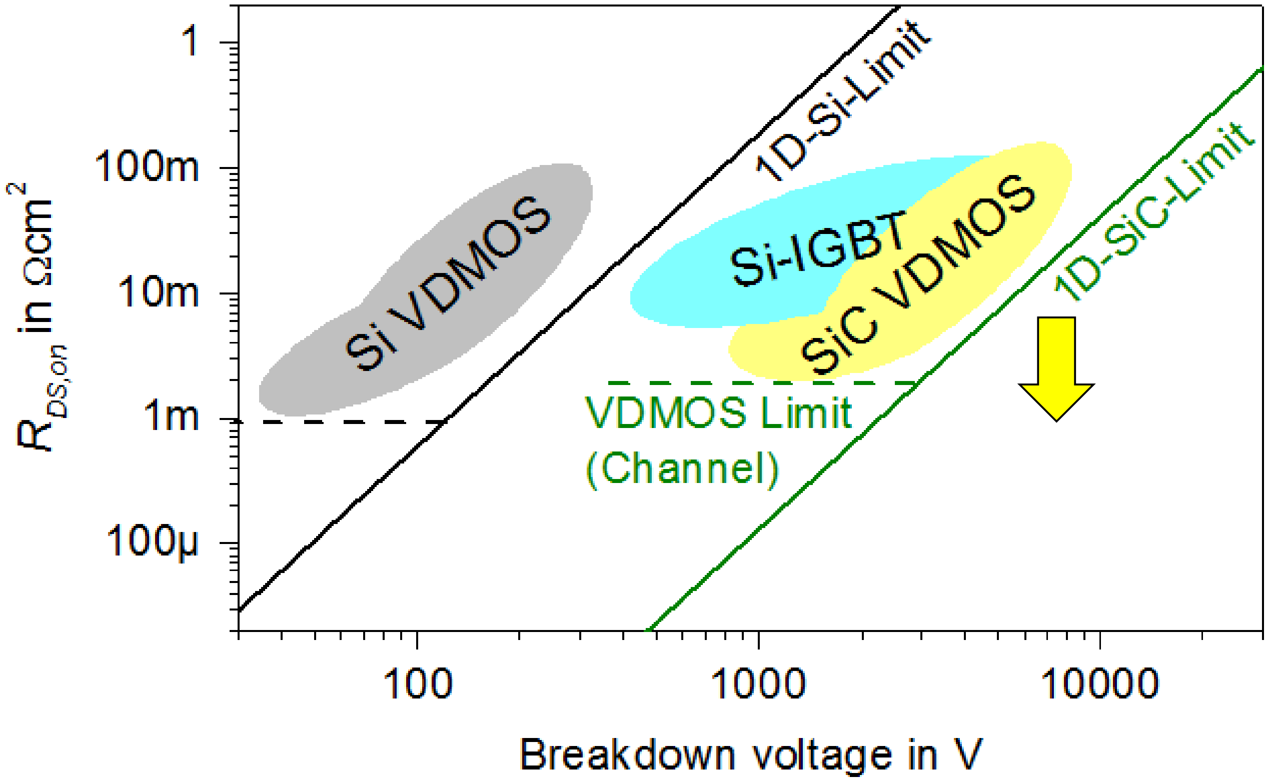
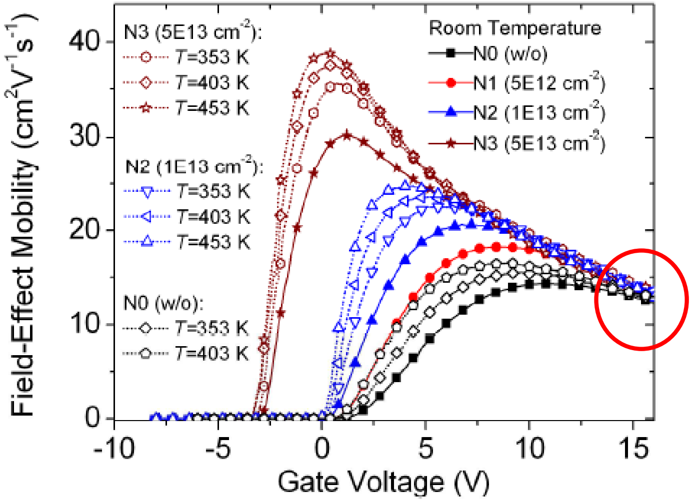
Evolution of SiC Power MOS technology

- Task 1: Reduction of On-State resistance to minimize die size/cost
  - Technology development depends on voltage rating



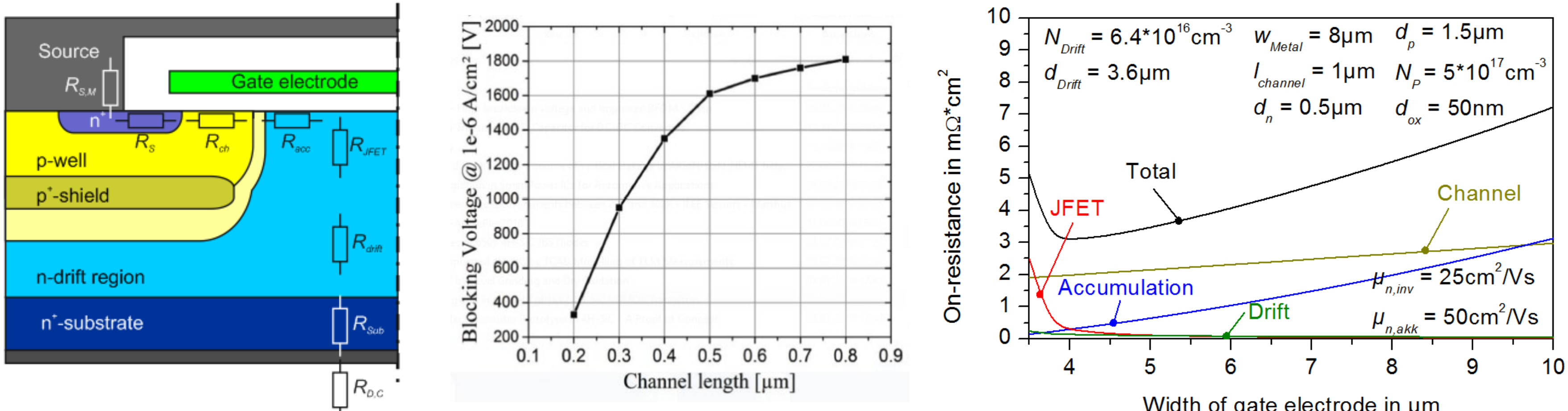
Evolution of SiC Power MOS technology

- Task 1: Reduction of On-State resistance
  - Improvements in channel mobility
    - Reduction of interface states by POA at 1300°C in NO
    - Channel mobility gradually increased to 20 cm^2/Vs at $V_{gs,max}$



Strenger et al., Mat. Sci. Forum 740–742 (2013), 537

  - Shielding of gate oxide required: p^+-shield
  - Shrinking of unit cell: e.g. reduced channel length, JFET implantation



H. Schlichting et al., Mat. Sci. Forum 963 (2019) 763-767

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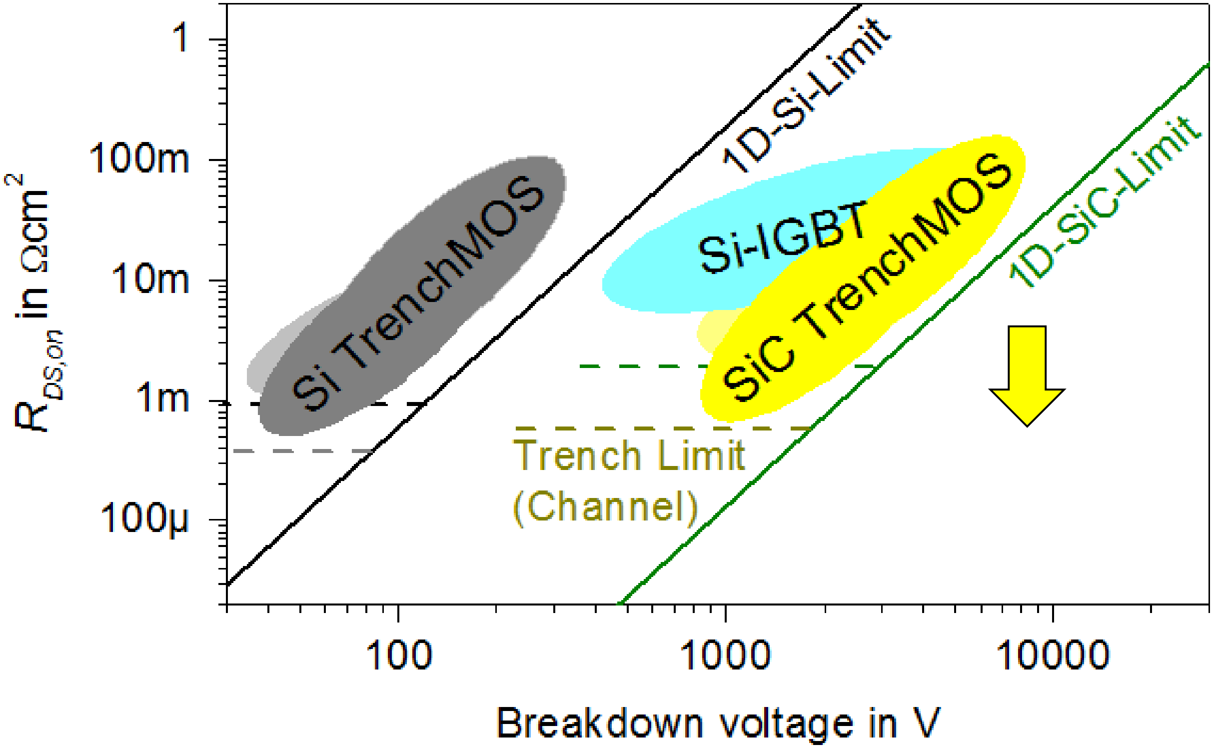
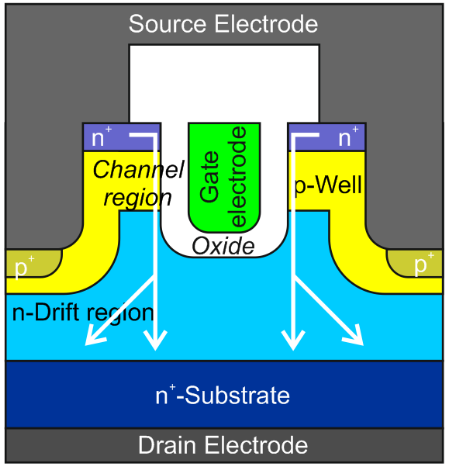


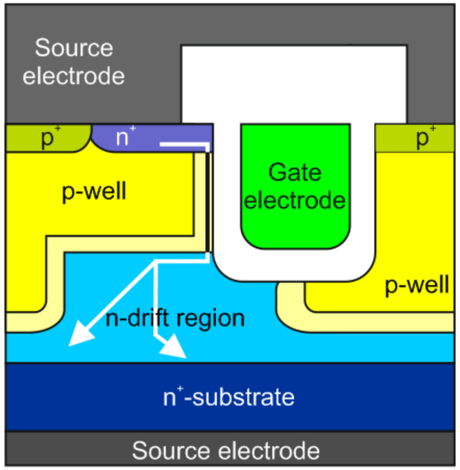
Evolution of SiC Power MOS technology

- Task 1: Reduction of On-State resistance
  - Implementation of trench gates
    - Increased channel mobility along (1 1 -2 0) orientation
    - Vertical channel → Pitch reduction compared to VDMOS
  - Shielding of trench bottom oxide vital!

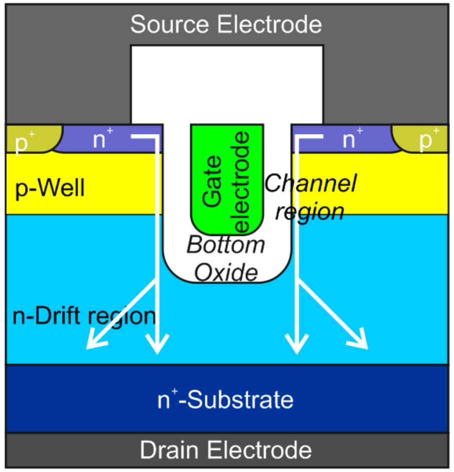
Examples of practical SiC Trench MOS concepts



Rohm / MaxPower Double Trench



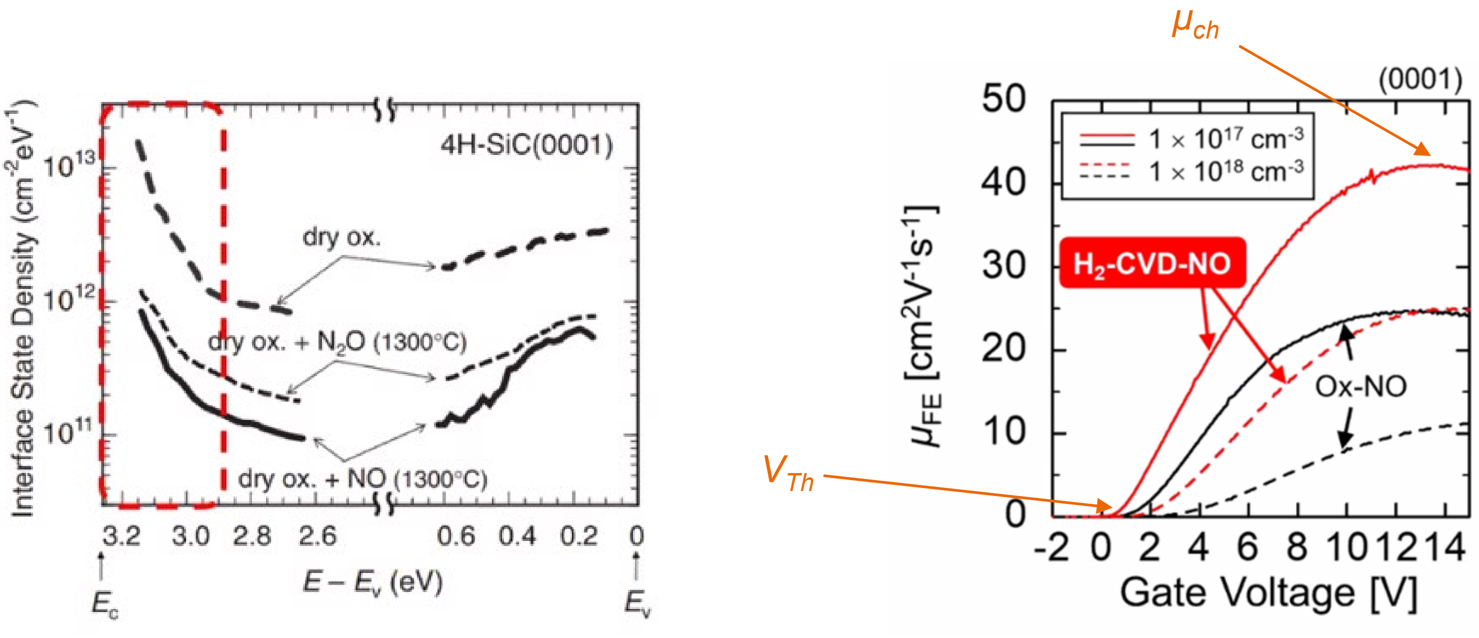
Peters et al., Power-Mag 3 (2017)



Banzhaf et al. MSF 858 (2016) 848-851

Evolution of SiC Power MOS technology

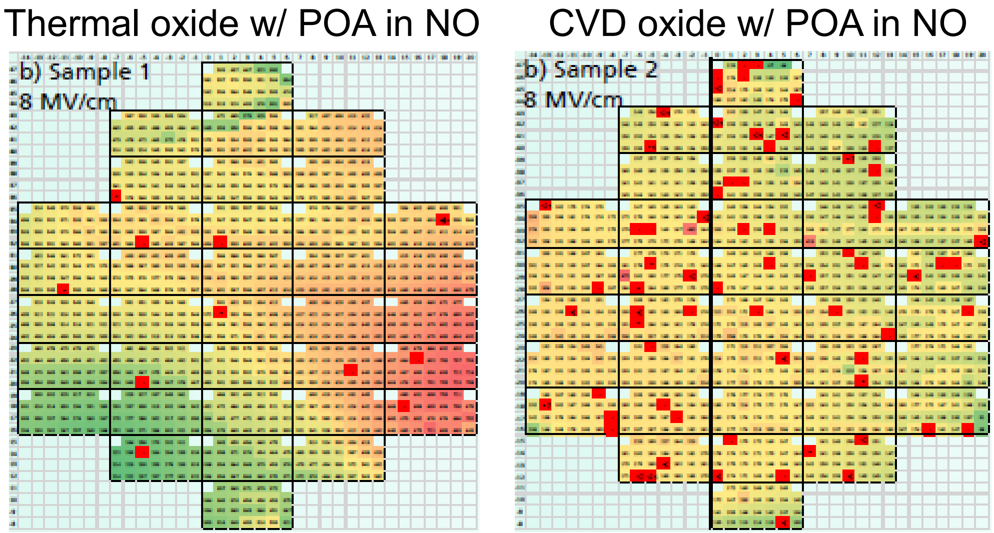
- Task 2: Design for Reliability, Manufacturability and Ruggedness
  - On-state resistance can be “traded off” to achieve application specific goals
  - Example: Gate oxide reliability
    - Choice of gate oxide affects channel resistance (thickness, mobility, V_{th} etc.)
      - Oxide capacitance & Maximum gate voltage



K. Tachiki et al., ECSCRM 2021

Evolution of SiC Power MOS technology

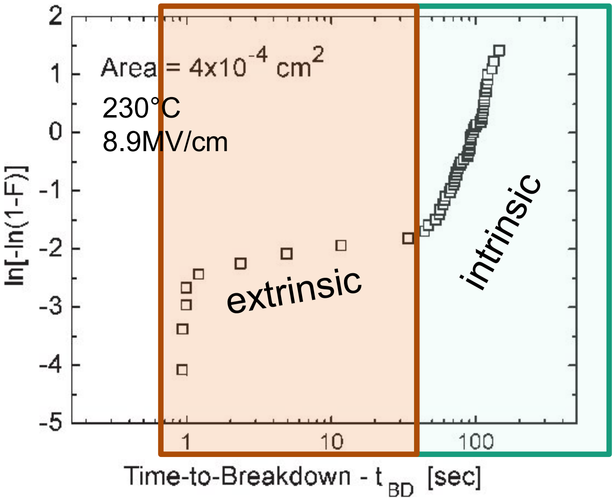
- Task 2: Design for Reliability, Manufacturability and Ruggedness
  - On-state resistance can be “traded off” to achieve application specific goals
  - Example: Gate oxide reliability
    - Choice of gate oxide affects channel resistance (thickness, mobility, V_{th} etc.)
      - Oxide capacitance & Maximum gate voltage
    - Gate oxide thickness also affects lifetime
      and Defect density, which can be traded-off against Yield (Burn-in)



Thermal oxide w/ POA in NO

CVD oxide w/ POA in NO

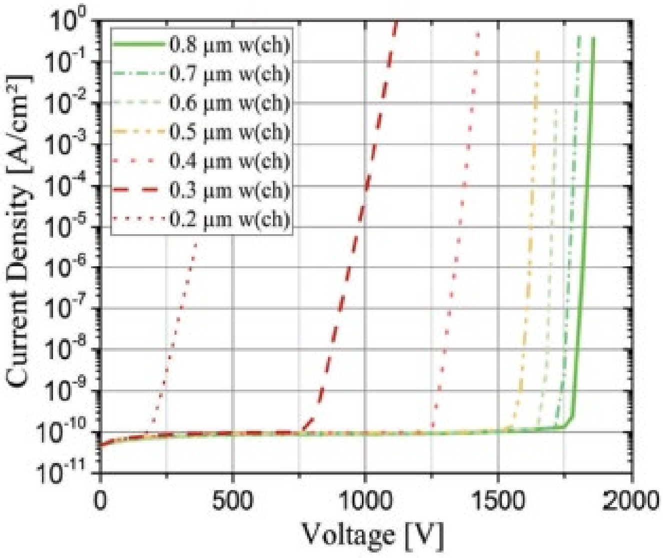
H. Schlichting et al., ECSCRM 2021

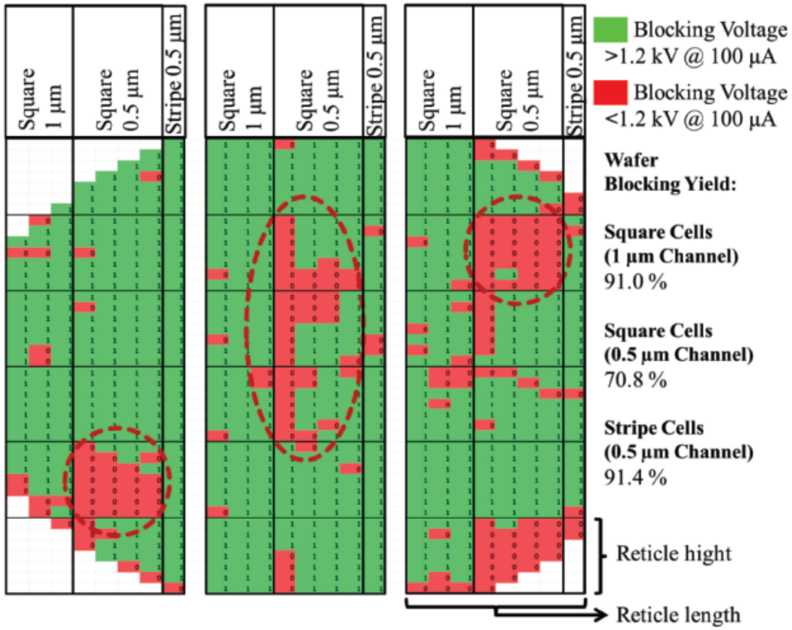


M. Gurfinkel et al., IEEE Trans Dev. Mat. Reliab. 8 (2009) 635

Evolution of SiC Power MOS technology

- Task 2: Design for Reliability, Manufacturability and Ruggedness
  - On-state resistance can be “traded off” to achieve application specific goals
  - Example: Integration density limited by overlay accuracy
    - Cell shrink minimizes on-state resistance → But lack of self-aligned gate process
    - Device variations and leakage currents emanate from overlay limitations
    - Self-aligned channel formation technique (additional processing effort)

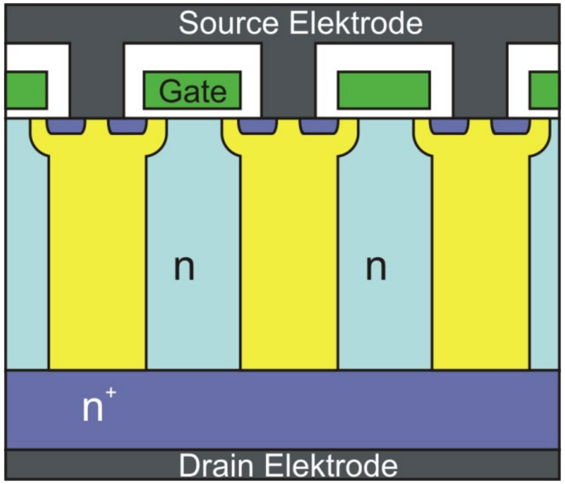


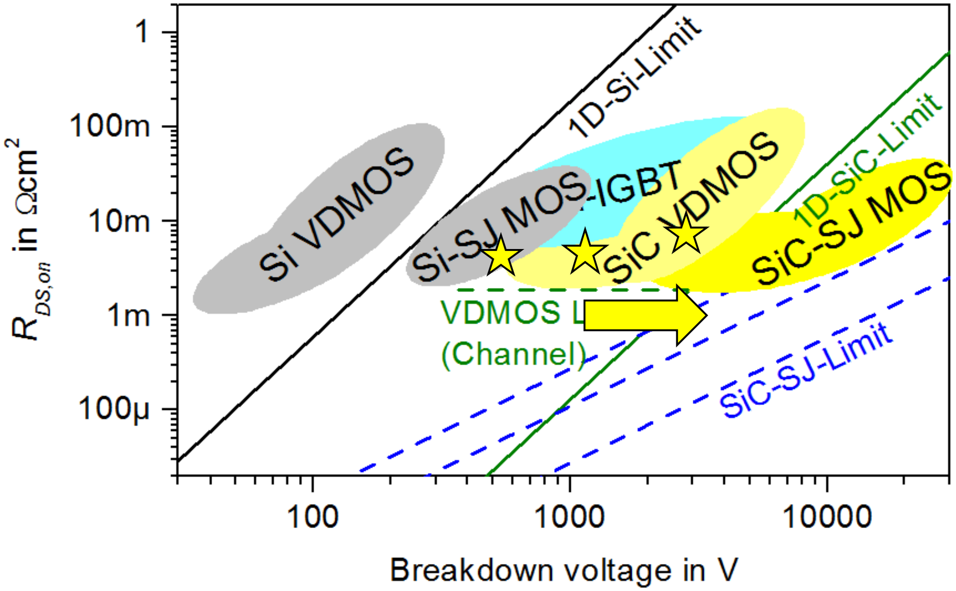


H. Schlichting et al., Mat. Sci. Forum 963 (2018) 763-767

Evolution of SiC Power MOS technology

- Challenges for further advancements
  - Unipolar high voltage devices
  - Superjunction device topology using vertical pillar structure (approx. 60µm @ 10kV)
  - Concepts (similar to Infineon / Toshiba solutions in Silicon):
    - Mid-energy ion implantation and epitaxial overgrowth (rinse & repeat)
    - High-energy ion implantation (e.g. filter implantation)
    - Deep trench etching and epitaxial refill





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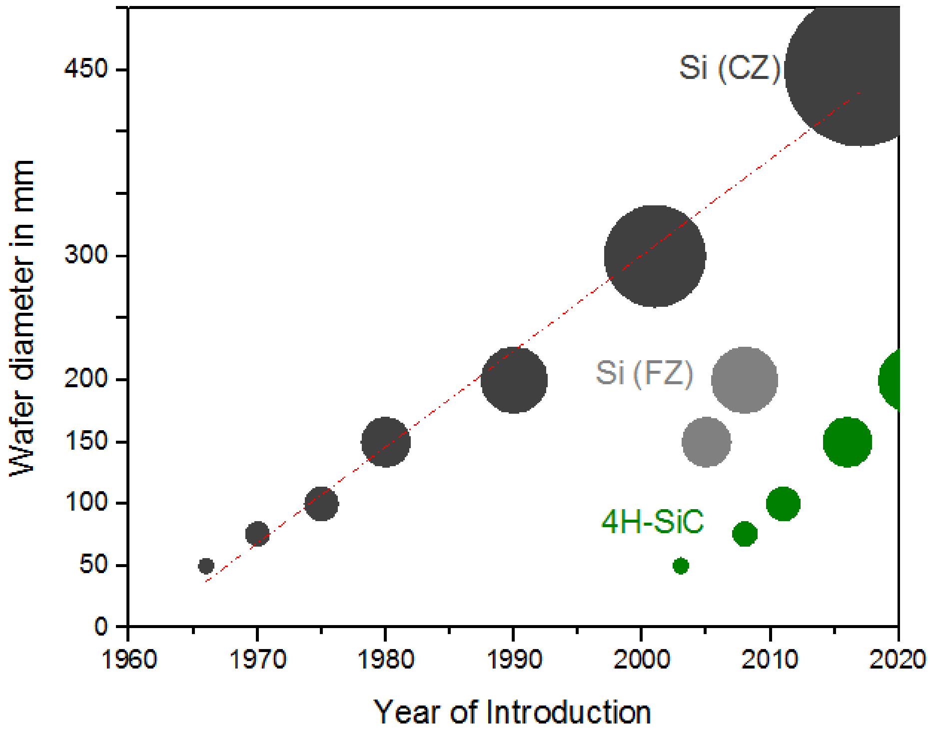
Possible goals for further tool optimization

- Challenges from device processing for fabrication tools
  - 200mm wafer diameter: SiC is on the go…
    - Significant cost in SiC is wafer substrate
    - Larger wafer size enables “double cost down” (per cm^2 wafer & processing)



Main drivers:

- Cost down
- Cost down
- 200mm Si-Fabs available
- Application pull

Main challenges:

- High defect density
- Growing larger diameters (Restart from scratch!)
- Control of wafer bow/warp

Possible goals for further tool optimization

- Challenges from device processing for fabrication tools
  - High temperature oxidation
    - Reliability issues for gate oxide, by defects induced by epitaxy or process.
    - Need for high reliability gate oxide → optimization of defect density
    - Investigations on long-term reliability required
    - Tool assessment and optimization for HT processing have to be established
  - Implantation and high-temperature annealing
    - Al and N as “new” dopants
    - Silicon implanters are feasible, high-temperature implantation as an addon?
    - High temperature annealing requires capping layer (typically carbon)
  - General requirements
    - Difficult handling of (200 mm) wafers due to warp/bow, need for high volume feasibility
    - Transparent wafers or “back to opaqueness” or both side-by-side?
    - Low manufacturing yield, especially for trench MOSFETs

Possible goals for further tool optimization

- Challenges from device processing for fabrication tools
  - Lithography requirements are very diverse, resolution is one, but not the only factor
    - Resolution, overlay and alignment accuracy
    - High exposure field size
    - High depth-of-focus
    - High energy dose for thick photoresist
    - Wafer warpage
    - Low costs / high throughput
  - Initial wafer thickness target is 500 µm in order to reach acceptable bow/warp
    - Transition to “standard” 350 µm (for 100/150mm) or even 200 µm is anticipated
  - Backgrinding / Wafer thinning is available with laser annealing of ohmic contacts
    - Temporary wafer bonding
    - Concepts similar to silicon (90µm IGBTs) feasible, manufacturability (line yield)?

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Opportunities and Conclusion

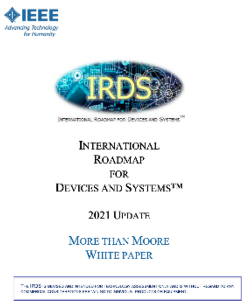
- Development of advanced SiC devices has just started
- Strong differentiation through performance, reliability, ruggedness trade-offs
  - System performance acts as guideline!

    Application specific solutions

    or

    Components-of-the-shelf?

- Not all technological solutions are known
  - Roadmaps in power electronics (like ITRS) are not publicly available
    - But industry (from tools to fabs) would benefit from clear routes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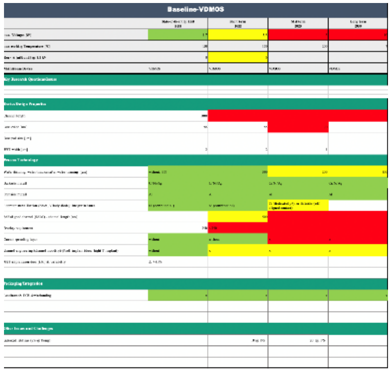
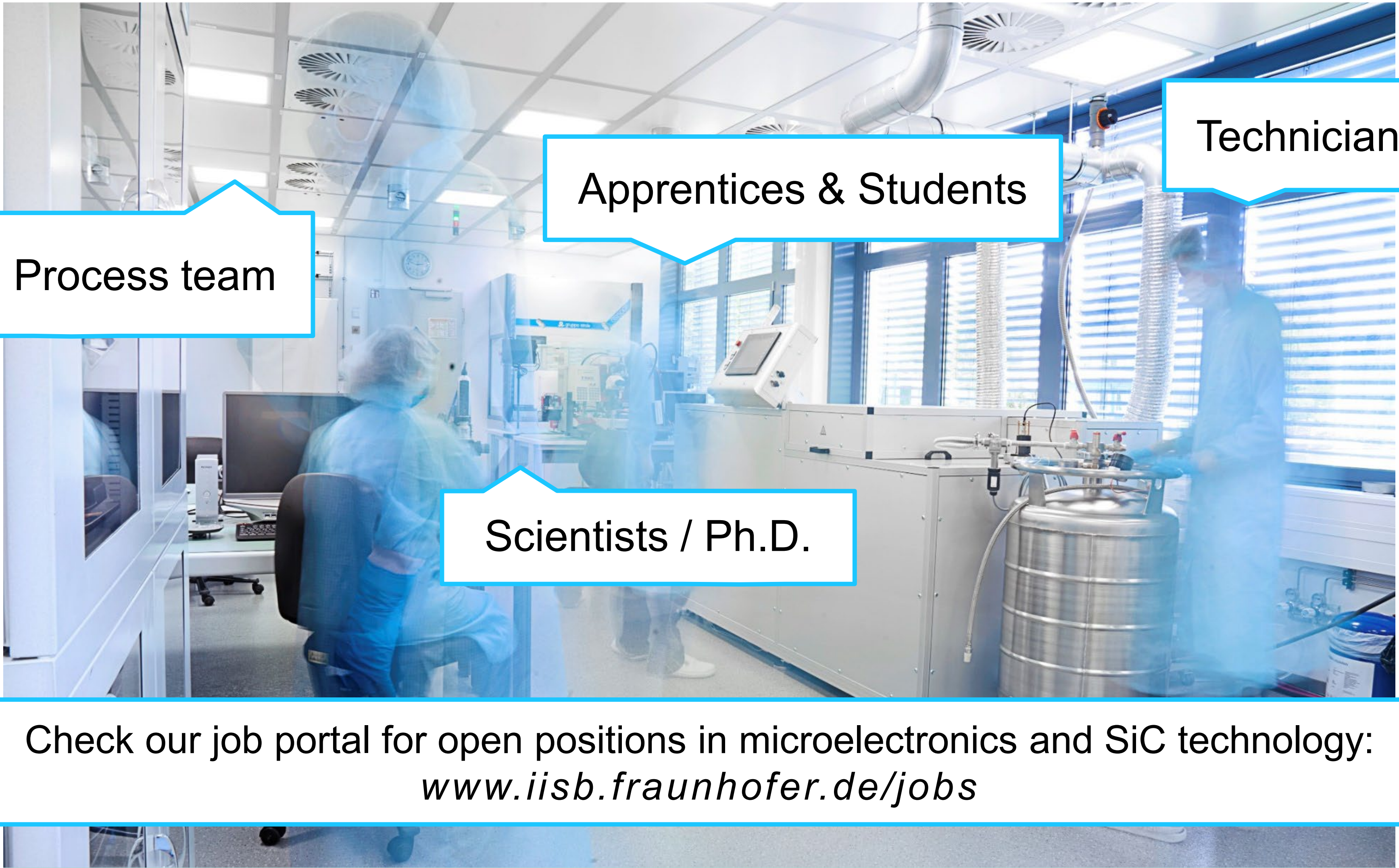


Spread the word: *We want you for SiC!*



Process team

Apprentices & Students

Technicians

Scientists / Ph.D.

Check our job portal for open positions in microelectronics and SiC technology:
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Thank you for Your attention!

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