Challenges and Opportunities in Semiconductor Packaging

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Semiconductor Industry

“It’s Never Been a Better Time”

Semiconductors: Key Enablers of the “Data” Era

PC ERA | NETWORK ERA | INTERNET ERA | MOBILE ERA | DATA ERA

Semiconductor Industry Revenue ($B)

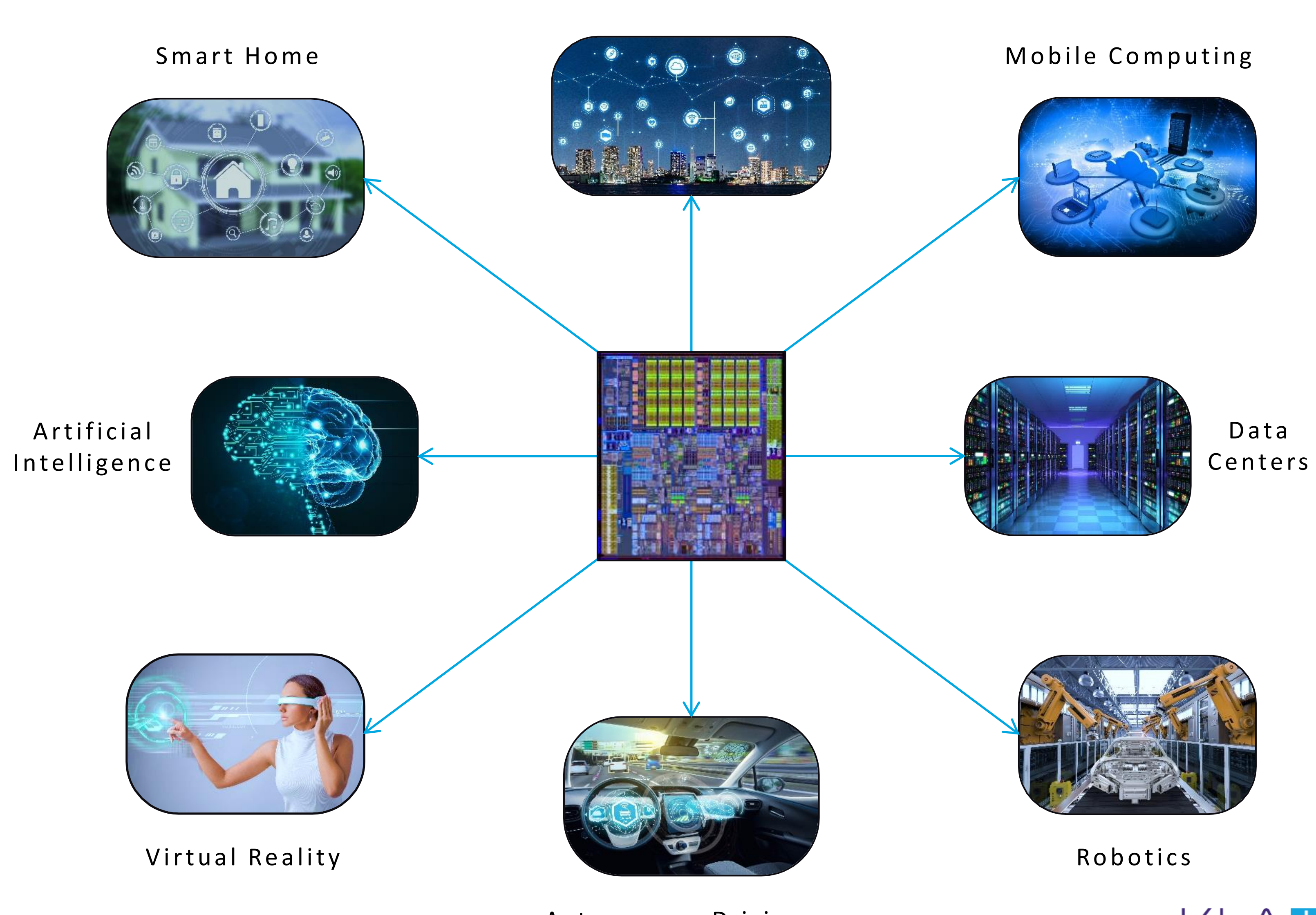
1990
2000
2010
2020

Sources: Industry data and Company estimates

The Data Era: Unprecedented Number of Market Drivers

The Data Era

everything becomes smart producing, storing, analyzing and transmitting an enormous amount of data



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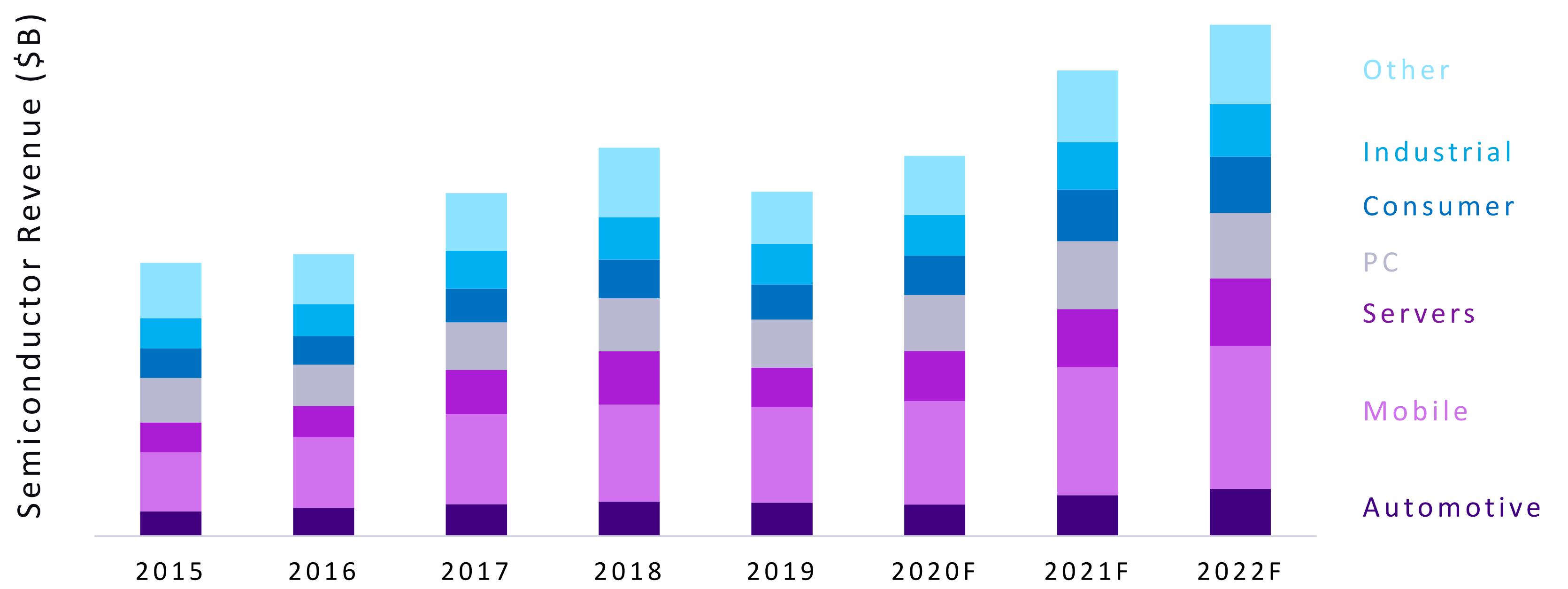
Semiconductor Drivers: The Secular Story Continues

Artificial Intelligence	5G Connectivity	Virtual Interaction	Mobile	Data Center	Automotive	Healthcare



Sources: Gartner

Semiconductor Technology Scaling for 50+ Years

1980 | 1990 | 2000 | 2010 | 2020

g-line (436nm) | i-line (365nm) | KrF (248nm) | ArF (193nm) | ArF Immersion (193i)

EUV (13.5nm)

1µm

500nm

250nm

130nm

65nm

32nm

16/14nm

10nm

7nm

5nm

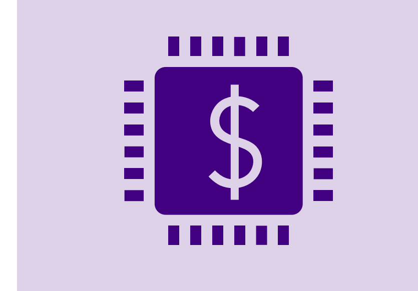
3nm

Conventional Scaling is Still Happening, But it Has Become Too Complex and Expensive

Advanced Packaging

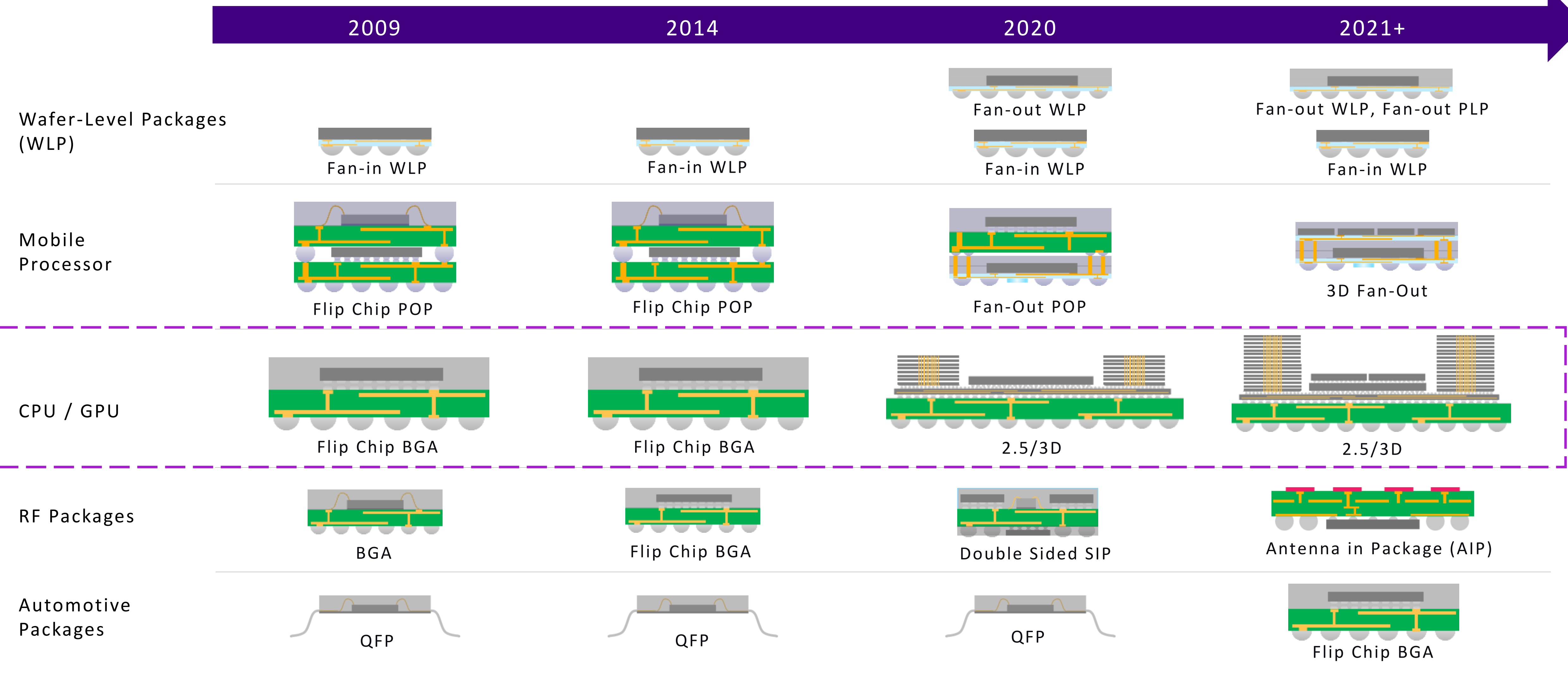
"Everything is Changing"

Advanced Packaging: Crucial to Semiconductor Technology Roadmap

Improved Bandwidth	Boost in Power Performance	New High-End Applications	Custom Form Factors	Increased Overall Si Area
				

From Device Protection to Performance Differentiation

Advanced Packaging: More Types | Higher Complexity



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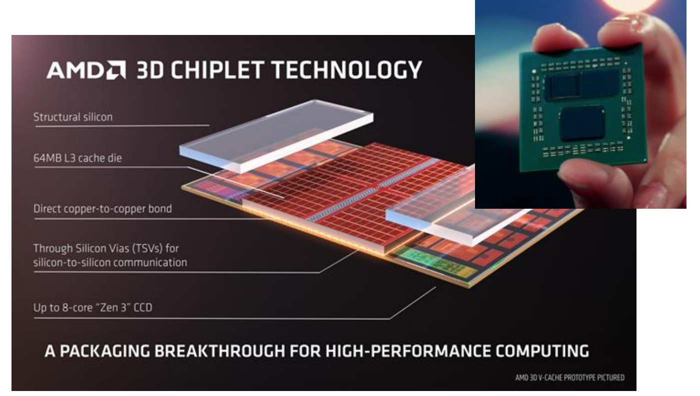
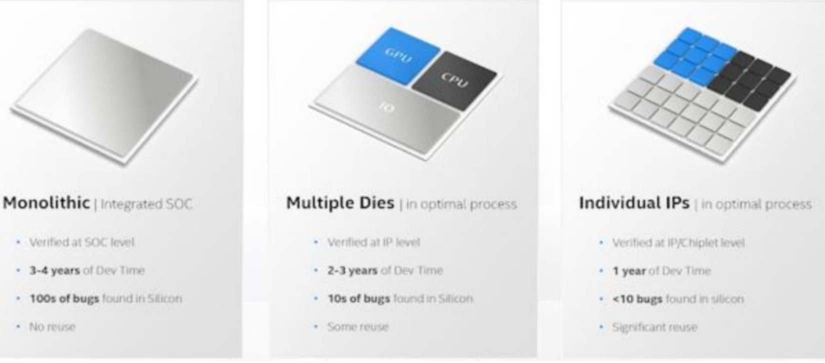
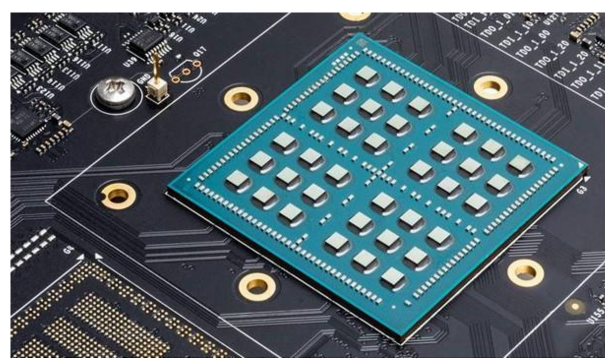
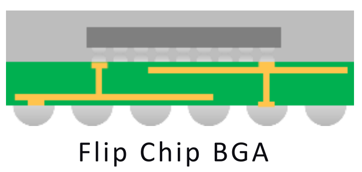
Chiplet Architectures

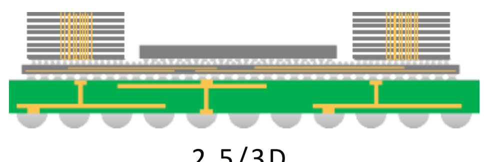




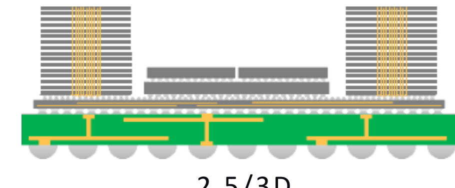




Flip Chip BGA



2.5/3D



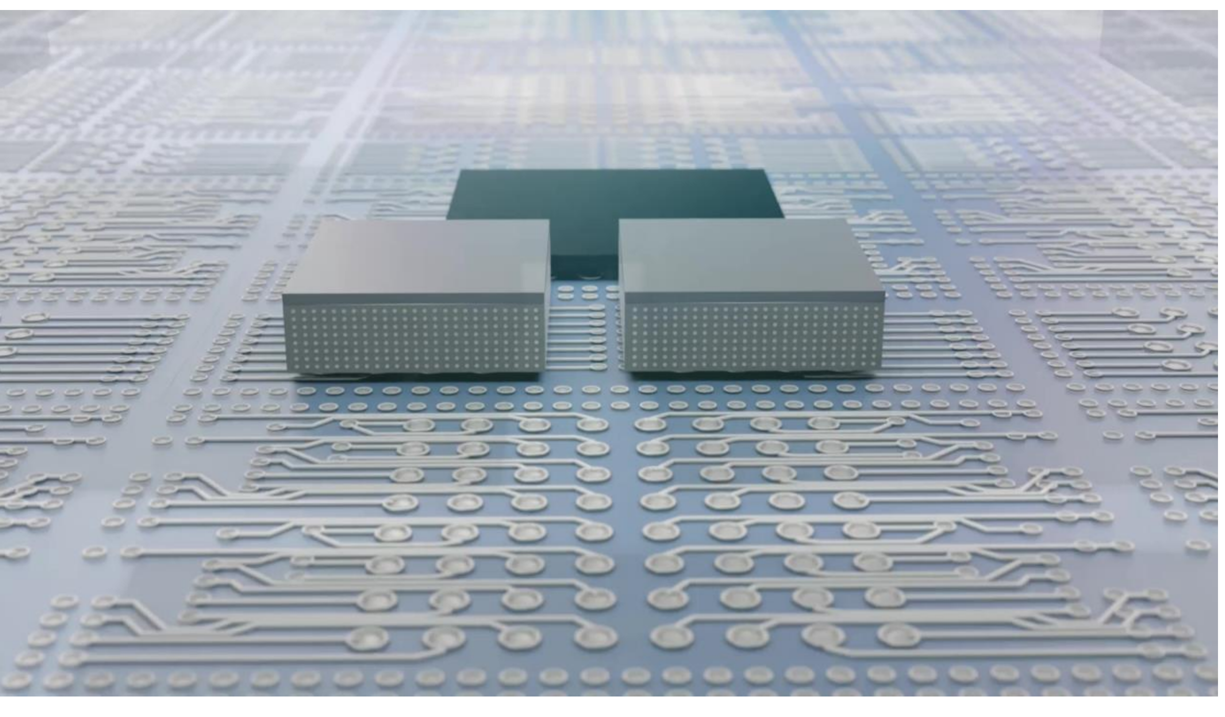
2.5/3D

 References: AMD Computex Keynote (July '21), Intel Architecture Day '20, and Nvidia (VLSI '19)

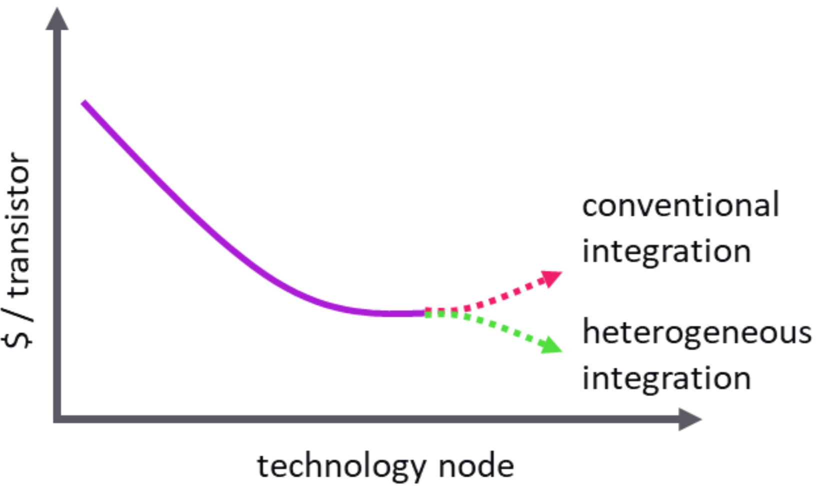
Heterogeneous Integration

“The Whole is Greater than then Sum of Parts”

Heterogeneous Integration: Scaling While Keeping Costs Down



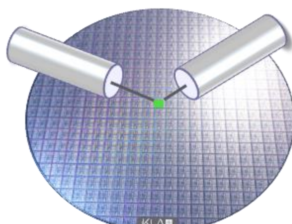
- From system on chip (SOC) to chiplets
- High cost only for core functionalities
- Disaggregation of the non-core functionalities
- Heterogeneous integration via packaging



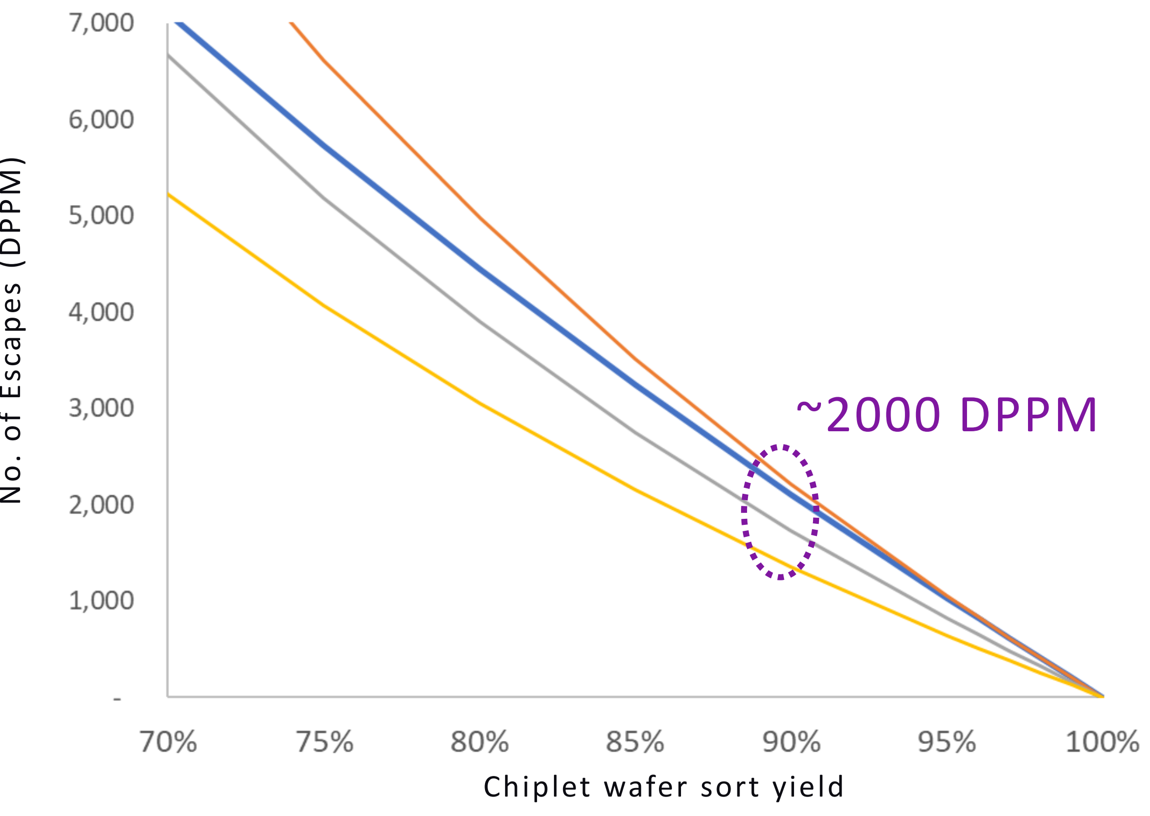
The Known-Good Die (KGD) Problem With Chiplets

How are defective chiplets escaping?

Function of fab yield and test coverage



Bare die test limitations



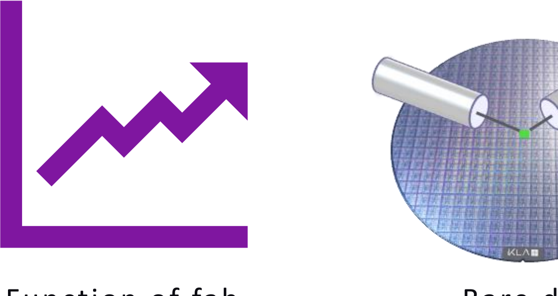
Number of Escapes Depends on Test Coverage and Yield

DPPM = defective parts per million

The Known-Good Die (KGD) Problem With Chiplets

Expensive challenge with increased die count

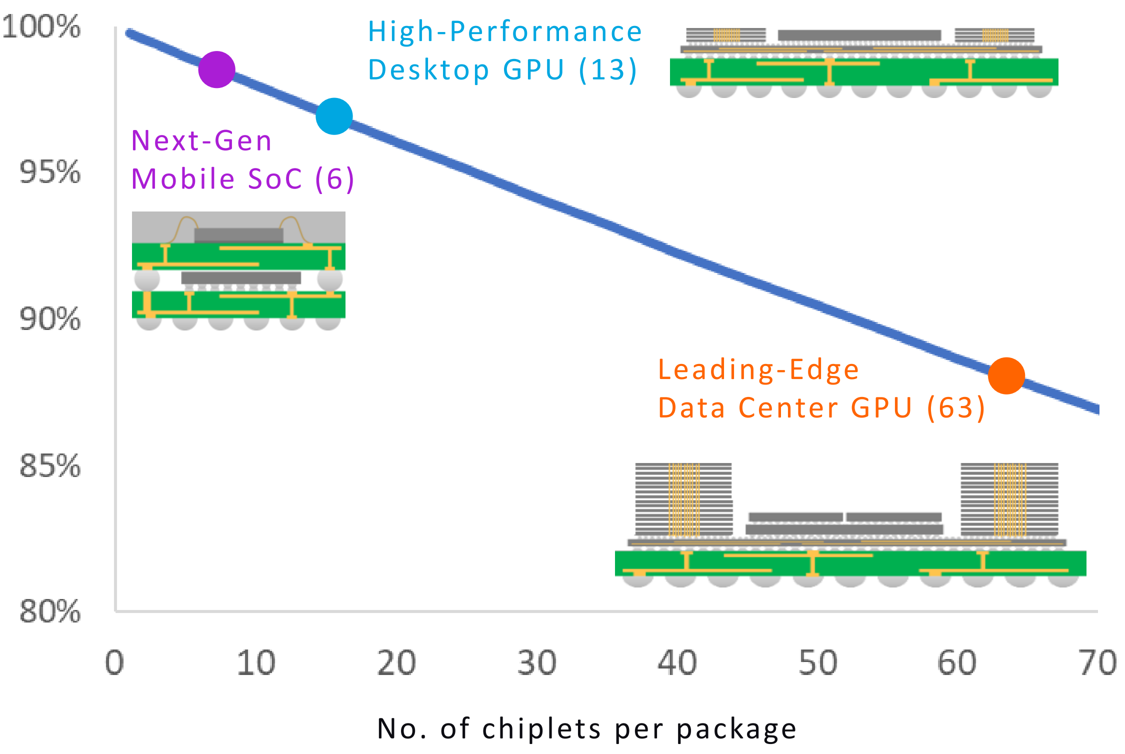
How are defective chiplets escaping?



Function of fab yield and test coverage

Bare die test limitations

Package yield @ **2000 DPPM** average chiplet escape rate



Package Yield Lower With Increased Number of Chiplets

DPPM = defective parts per million

Chiplet Escape Reduction Requires a New Approach

Chiplet Escape Reduction	
100% of lots, 100% of die on critical layers	Inline optical inspection screening for early identification of at-risk devices
	Improved wafer sort (including µbump probing)
wafer probe	More sophisticated electrical test binning

Inline defect screening methods already reducing escapes for automotive chips

I-PAT® (Inline Defect Parts Average Testing)

Inline wafer inspection → I-PAT analysis of inspection attributes → Statistical outlier analysis → High risk die identified and screened

Methods to Improve Quality and Reliability for Auto Chips Can Also Improve Chiplet Package Yield

Hybrid Bonding

Innovative Technology for Heterogeneous Integration

Hybrid Bonding: The Next Inflection in Heterogeneous Integration

Integration Schemes

a
Logic (memory)
Logic

b
Logic (memory)
Logic

c
Logic (memory)
Logic

d
Sensor
HV
Logic (memory)
Logic

Source: tsmc

Thermo-Compression (Bump)

Source: tsmc

Hybrid (Bump-less)

Source: tsmc

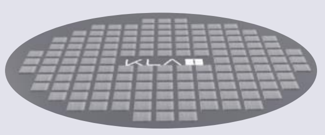
- Key Benefits: Speed, Bandwidth and Power Efficiency through increased interconnect density
- Hybrid Bonding in Packaging with D2W integration key for AI Logic Chips and High Bandwidth Memory

Several Inspection, Metrology and Integration Challenges

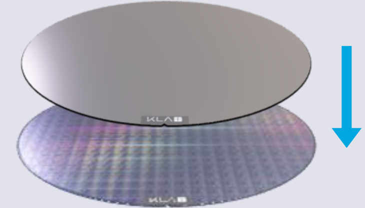
Die to Wafer Hybrid Bonding Integration Schemes

Collective Hybrid Bonding

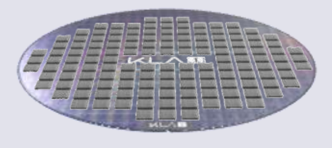
Die to be bonded are prepared, diced, then placed on carrier wafer



Activation, cleaning and then bonding



Remove carrier wafer, leaving bonded die on target wafer

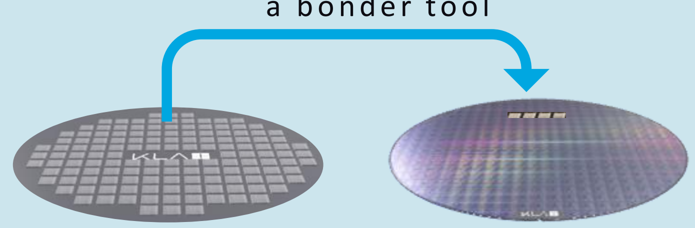


- Die transfer all at once
- Narrow die thickness range
- Proven die activation and cleaning methods
- Possible rework
- Challenges include thin die, cleanliness, alignment, carrier removal

Sequential Hybrid Bonding

Singulated die are transferred to carrier for activation and cleaning

Direct placement of die using a bonder tool

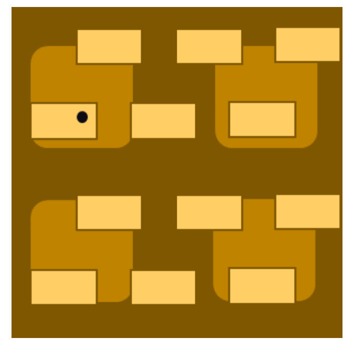


- Die transfer one by one provides flexibility
- No die thickness limitations
- Challenges include handling of multi-die stacks, die activation and cleaning, alignment, cleanliness

Hybrid Bonding Challenges

Surface Cleanliness Before Bonding

- Significantly cleaner surface required compared to thermal compression bonding (TCB)
- Particles/residues cause voiding

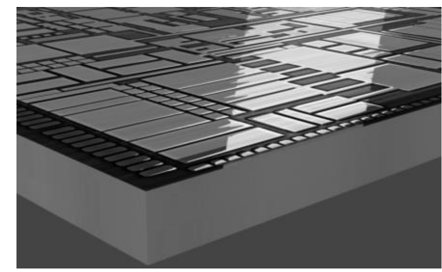


Surface Topography Before Bonding

- Cu/dielectric profile critical
- CMP process control
- Current AFM not capable in high volume manufacturing

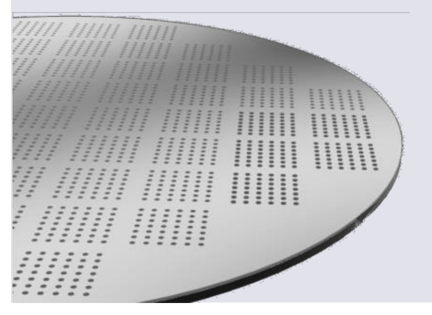
Die Singulation Cleanliness and Final Profile

- Conventional die singulation (laser/saw) very dirty
- Bonding and stacking very sensitive to die profile

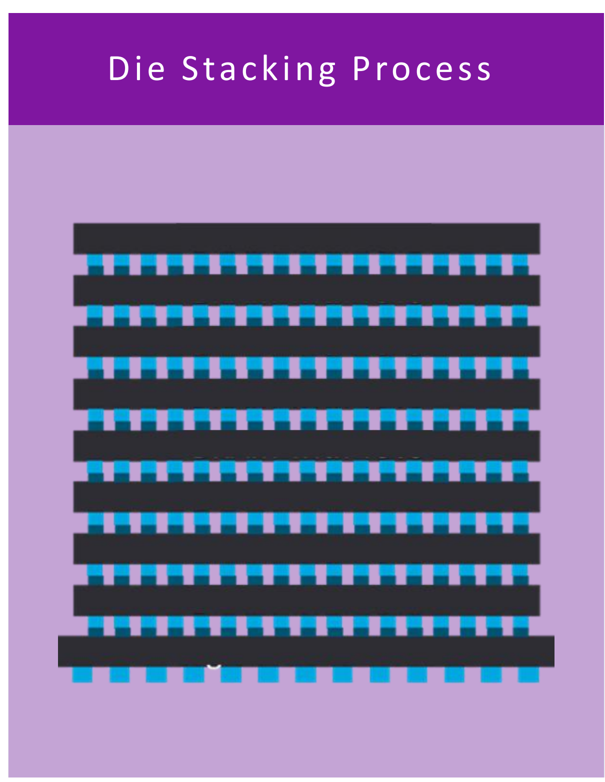


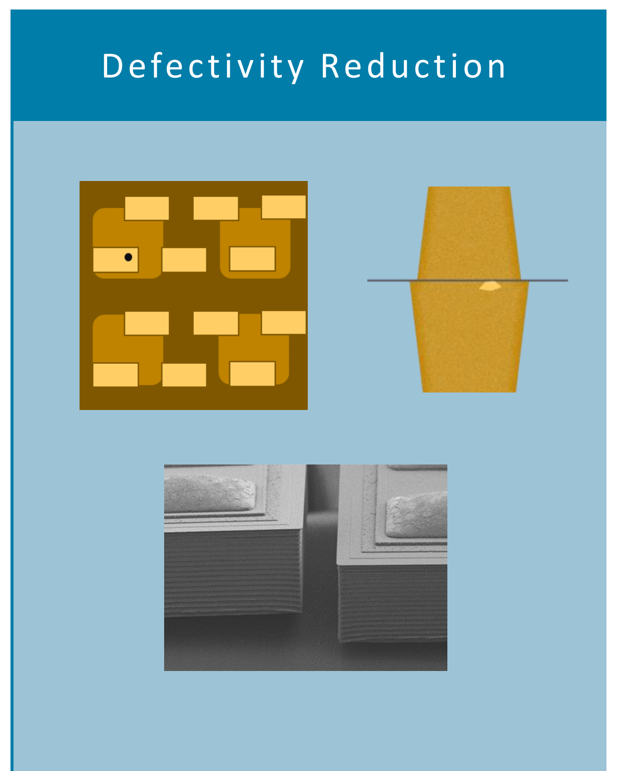
Low Temperature Processing

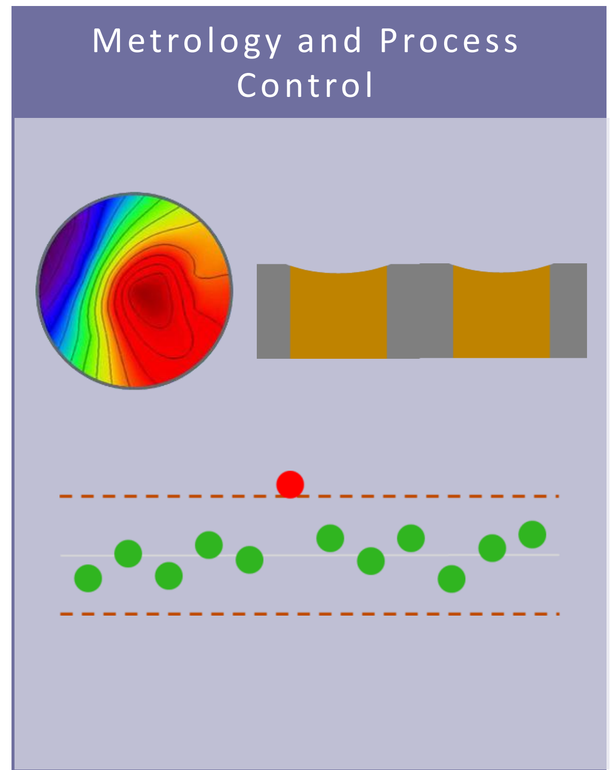
- Etch/deposition processes on the presence of soft adhesives
- High-quality but low temp (<125°C) processing capabilities needed

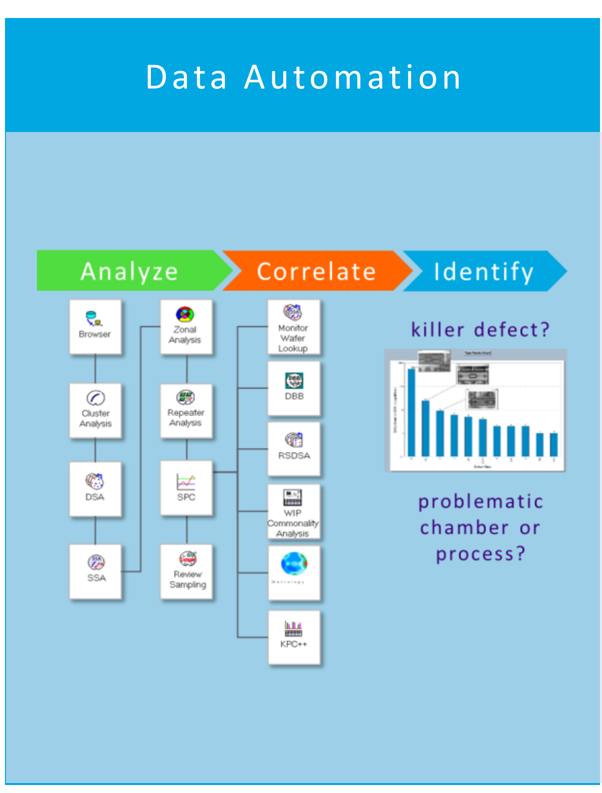


Collaborations: Key to Tackle the Challenges and Provide Solutions







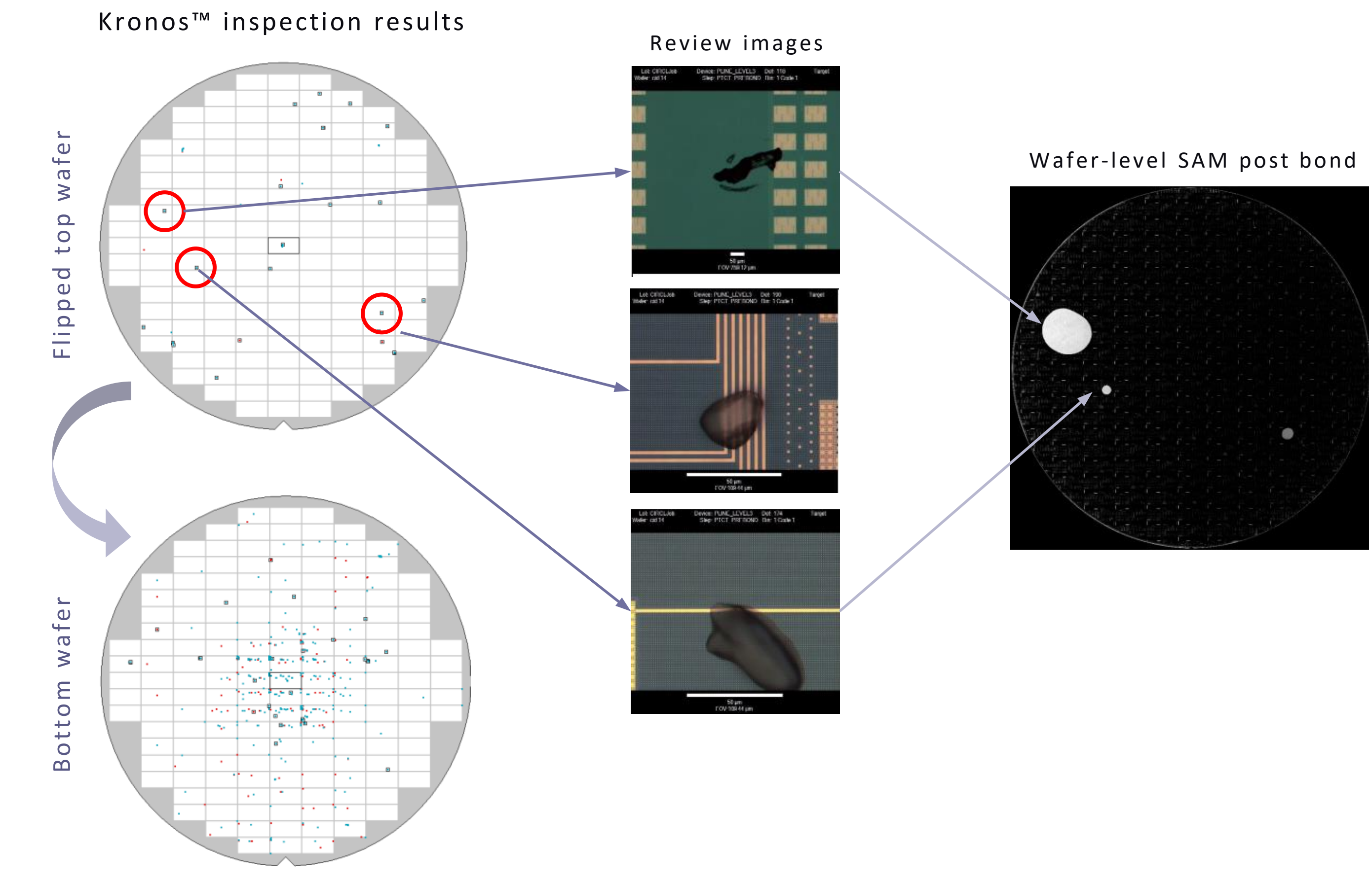


Several Active Projects with Top Semiconductor iDMs, Foundries and OSATs

Surface Cleanliness Before Bonding

Wafer Inspection Requirements

- High sensitivity for 3DIC and FO
- Detect and resolve excursions
- Bonded, thinned, warped and diced wafers



Post-Bond Void Correlation to Defects

FO = fan out
TSV = through-silicon via

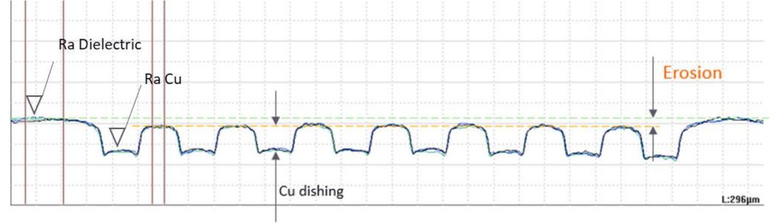
Source: imec, SEMICON Korea 2017
SAM = scanning acoustic microscopy

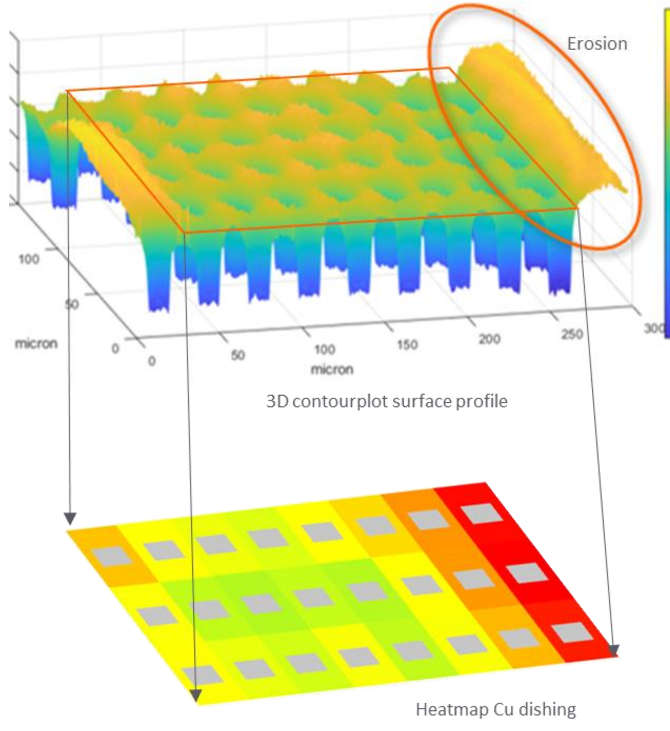
Surface Topography Before Bonding

Metrology Requirements

- Surface profile for hybrid bonding
- Si thickness for TSV process control
- Final revealed TSV height

Erosion and Cu dishing in Zeta cross section





Quantify Erosion, Cu Dishing and Roughness

Die Singulation Cleanliness and Final Profile

Dicing Requirements

- Increased die strength
- Defect free dicing
- Reduced dicing kerf width

Wafer-level SAM post bond

	Defects	Optical image	Wafer-level SAM post bond
Plasma Dicing	286 defects (1µm and above)	Optical image shows smooth edge	No voids
Blade Dicing	19,000 defects (1µm and above)	Optical image shows rough edge	Voids

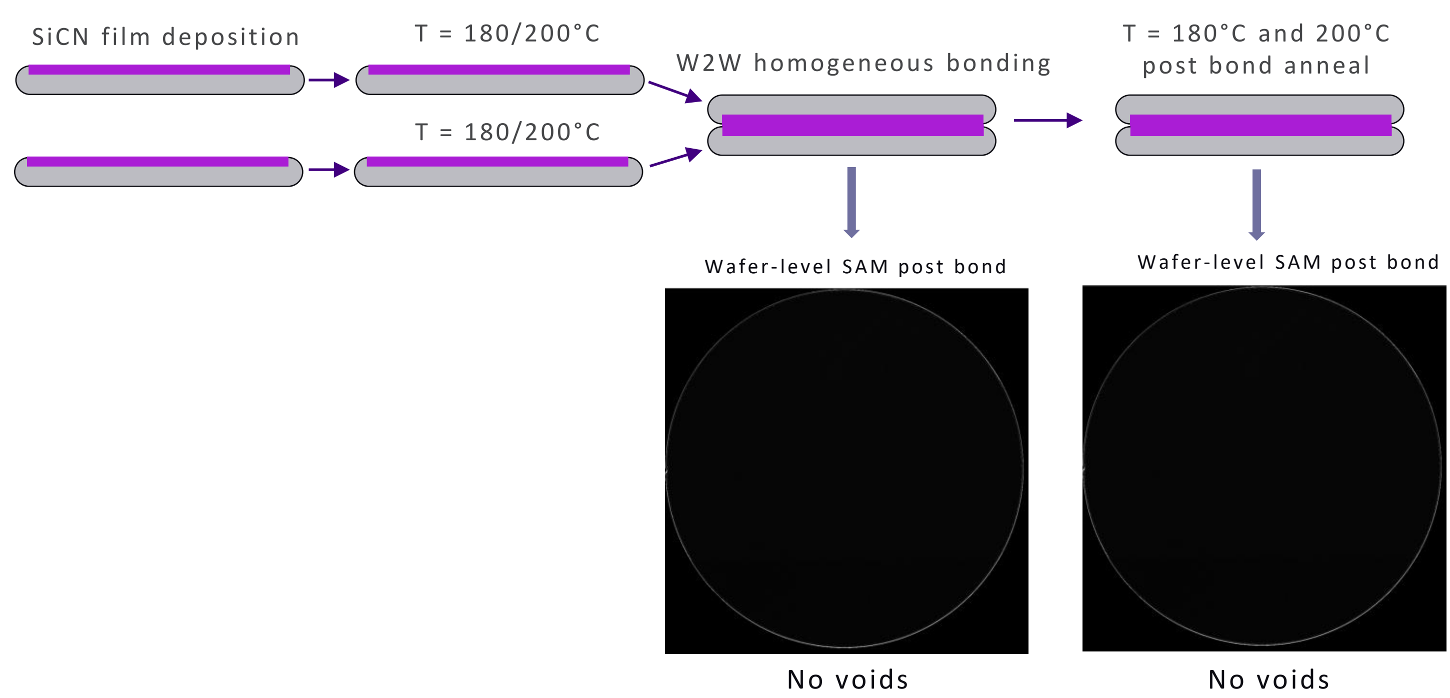
Plasma Dicing Results in Smooth Profile and Low Defectivity

Source: collaboration with imec

Low Temperature Processing

Low Temp PECVD Requirements

- SiCN films at 175°C and 350°C
- Tunable carbon and stress
- Good thermal stability
- Void free

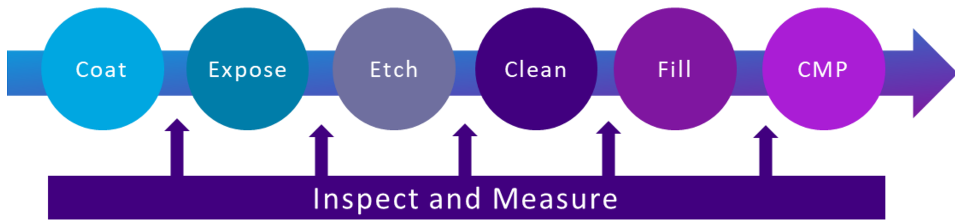


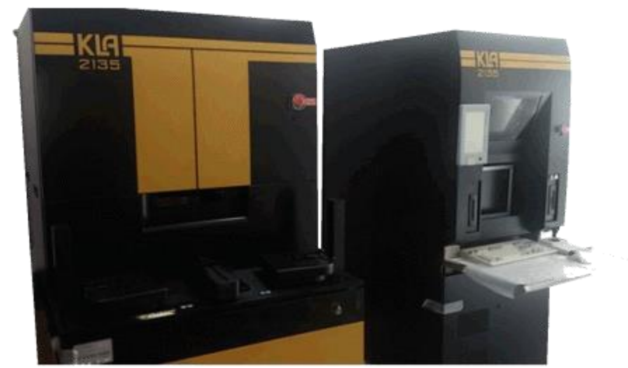
Low Temp SiCN Films are Void Free After Bond and Anneal

Source: collaboration with imec

Data Automation Solutions

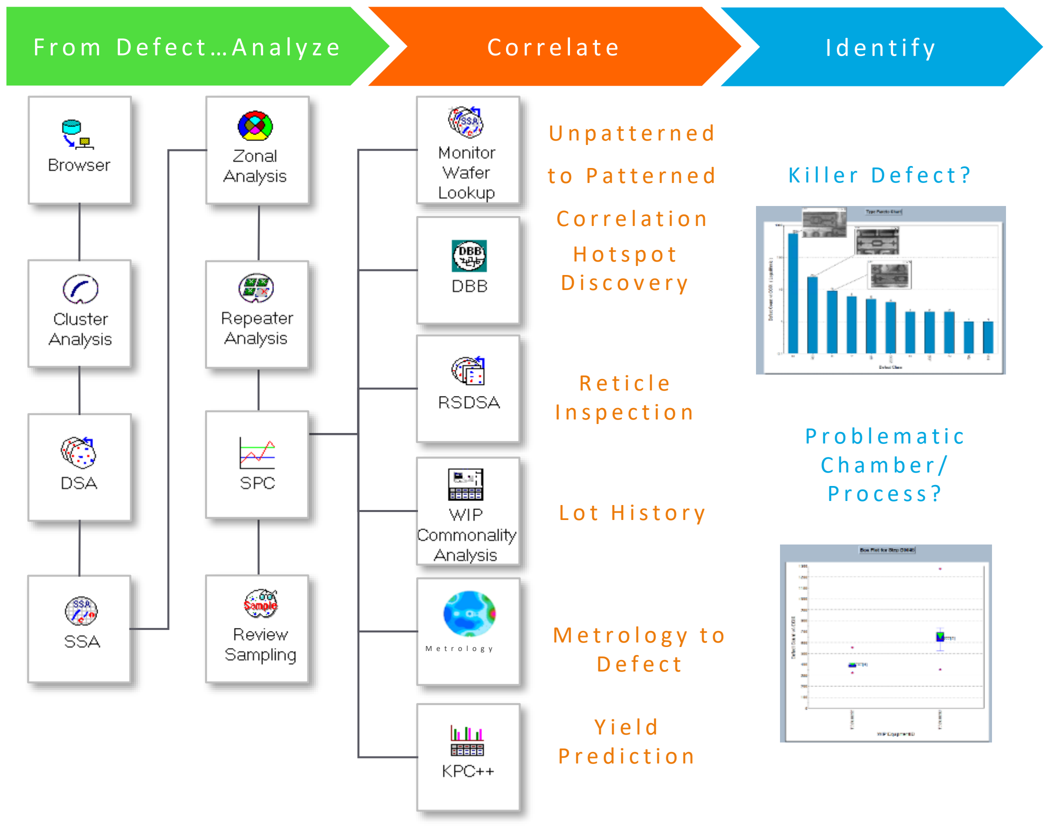
Process Control





Introduced in frontend in mid 90's

Klarity® Data Analysis System

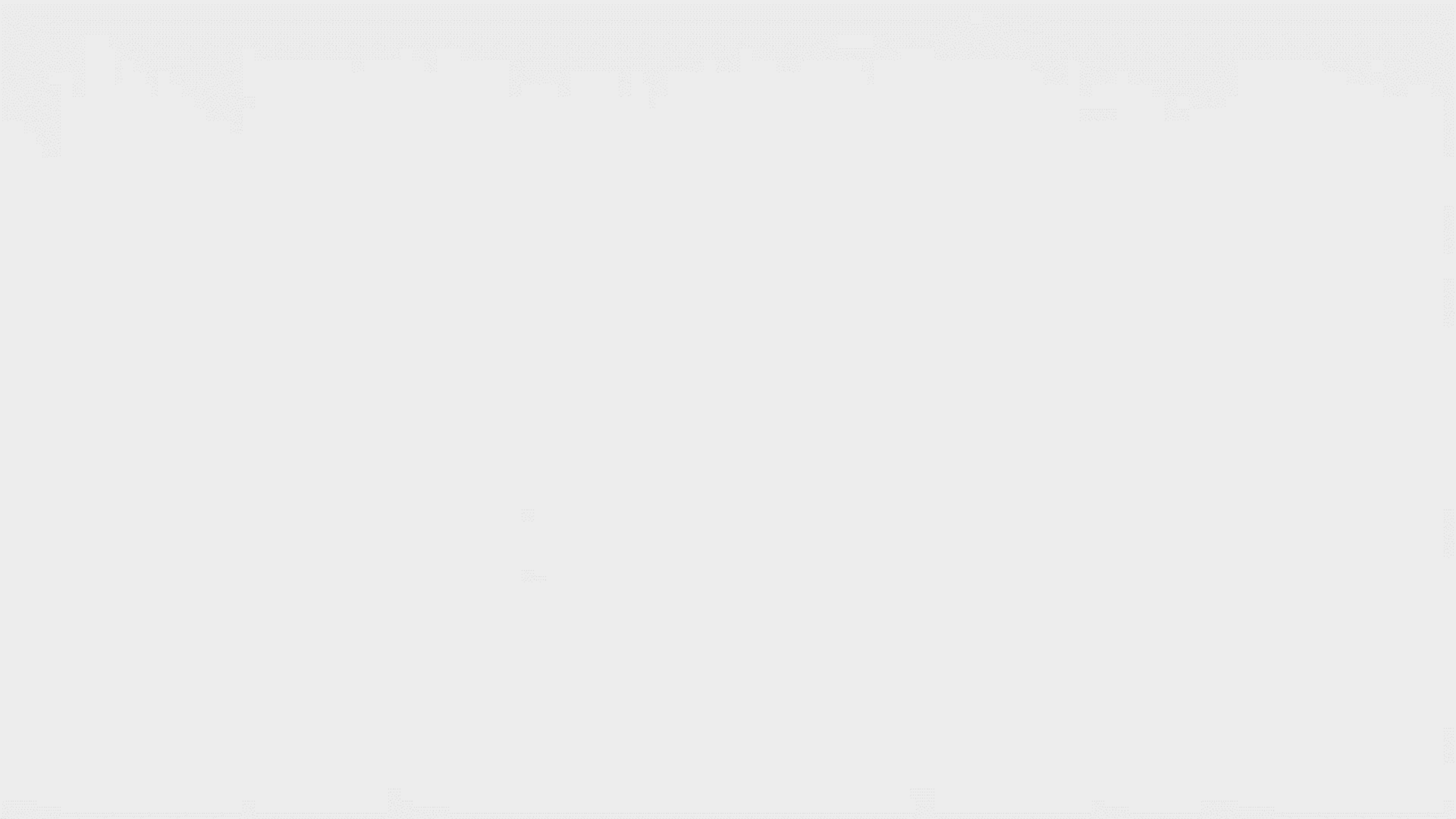


Summary

An Exciting Time for Advanced Packaging

An Exciting Time for Advanced Packaging

- Packaging is driving performance differentiation
- Heterogeneous integration enables scaling
- Chiplets require Known Good Die; established methods from auto fabs can help
- Hybrid bonding technology is driving innovation for both process and process control



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Thank You

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